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Distributed Generation System using Parallel Inverters Supplied by Unstable DC Source

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Abstract: This study presents the analysis and design of distributed generation system. The system consists of a full-bridge DC-DC converter, two units of three-phase inverters connected in parallel and a controller. Two units of conventional three-phase DC-AC inverters connected in parallel with series resistors were added to the inverter output to maintain the same current in each inverter and to minimize the circulating current in the parallel inverters. High frequency third harmonic injection PWM (THIPWM) was employed to reduce the total harmonic distortion and to make maximum use of the DC bus voltage. The generation of control algorithm for three-phase inverter is implemented in Digital Signal Processing (DSP) boards. The THIPWM have been done such that the inverter output voltage is synchronized with the grid voltage thus making the inverter suitable for grid connection. The three-phase inverter operates with a total harmonic distortion of less than 2% on output voltage and current signals. Experimental results are shown validate the proposed system. A full distributed generation system has been implemented and tested, the testing of the system proves that the system operates with minimum circulating current on the parallel connected inverter and minimum harmonic distortion on the inverter output voltage and current.

Key words: DC/DC converter, inverters parallel connection, third harmonic injection PWM, distributed generation

INTRODUCTION

Distributed Generation (DG) have become increasingly more accepted since the demand for reliable and secure power systems with high power quality increases, especially after producing alternative energy resources (such as fuel cell, wind-turbine, bio mass, micro-turbine and solar-cell systems) with lower costs (Nigim and Hegazy, 2003). To connect any of Distributed Energy Resources (DERs) to the existing three-phase, power systems effectively and efficiently, power electronics-based power conversion systems need to be developed to deliver a proper energy (Marei *et al*., 2004). Through the control of the power conversion system, benefits such as increasing reliability, security and fewer downtime can enhance the utility grid without replacing the existing transmission and distribution system.

The concept of DG has recently become commercially extensive. Distributed generation is the interconnection of alternative energy resources to the utility grid system close to the load point to alleviate the demand and expansion of the electric transmission system (Daly and Morrison, 2001; Puttgen *et al*., 2003). DG is meant to shift the structure of the utility system from a centralized, radial system to energy source connected on the distribution level. The penetration of distributed generation into the energy market has some advantages including (Nigim and Lee, 2007; Hammons, 2007):

- Distributed generation reduce the dependency on fuel sources.
- Enable renewable energy usage which has minimum impact on the environment and it offers free replacement of prime fuel sources.
- Electrify the rural areas, which give chance of development for those areas.
- Reduce the need for transmission lines extension or construction and it can be used to support demand during peak period (Grijalva and Visnesky, 2005).
- Effects power management concept that utilizes local resources nationally.

There are two basic types of distributed energy resources: DC and AC voltage producing sources (Wang *et al*., 2004). For either type to be connected to the utility system their outputs need to be processed to match

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the utility. DC voltage producing source include fuel cell and solar cell array. However, these are low voltage sources. The processing for both of them includes the use of DC/DC converter to boost the DC voltage to a higher level. A storage element is needed at the high voltage DC bus. The DC voltage is then converted to three-phase grid voltage. AC voltage producing source includes micro-turbine and wind turbine. The micro-turbine produces AC voltage with high frequency which needs to be rectified and then converted to the grid frequency and voltage. In this case a storage element is not needed. Wind turbine produce variable frequency AC which needs to be rectified to supply storage element and inverted to three-phase grid voltage and frequency.

Several types of distributed generation system have been reported in literature (Kwak and Sul, 2006; Marwali and Keyhani, 2004). Most of the systems proposed in the literature discussed the control strategy of the distributed generation. To improve the power capability of the inverter, parallel inverters are required (Cai *et al*., 2008). The relatively low switching frequency may increase the current harmonic in the output current of the inverter. The THI PWM method to control the power factor of the inverter output current is used in grid connected system. However, it is very difficult to generate the correct third harmonic amplitude (Naik *et al*., 1995). The proposed system in this study used two units of parallel inverter with THIPWM switching technique. The 5 kHz switching frequency created accurately using DSP which make the power factor approximately unity. The use of low value series resistor could balance the current in the inverters without affecting the inverter efficiency.

THE DC-DC CONVERTER CONFIGURATION

The proposed DC-DC converter is shown in Fig. 1 consists of H-bridge inverter, high frequency transformer and full-bridge rectifier. Four IGBT switches were used to construct the mentioned H-bridge inverter. A high frequency transformer is used to step-up the square wave voltage produced by the H-bridge to the required voltage level. The transformer provides isolation between the DC source and the three-phase inverter. The saturable inductor L_{IK} with the blocking capacitor C_R allowing lagging-leg switches to be turned off with ZCS. Full bridge rectifier connected to the secondary side of the transformer to convert its voltage back to DC voltage. L_f and C_f used as filter to the output DC voltage.

The converter operates in a mode that provides Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) for the active switches. The gating signals are

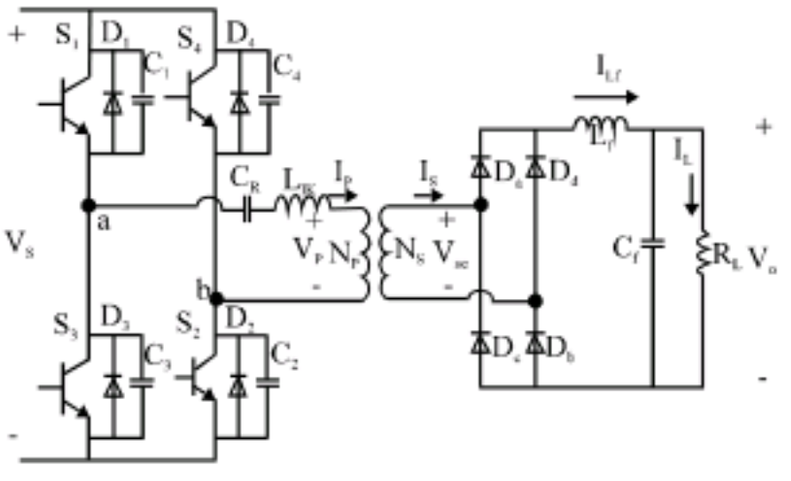

Fig. 1: DC-DC converter circuit diagram

turning on the crosswise opposite switches in the bridge simultaneously, a phase-shift PWM is introduced between the switches in the left leg and the switches in the right leg. The switches overlapping determine the converters duty cycle (Ma *et al*., 2005).

Converter analysis and design: The dead time between S_2 and S_4 has to be set at t_d to ensure sufficient time to charge and discharge the capacitances which given during the maximum possible load. The time t_d can be determined as:

$$t_d = V_S \frac{C}{nI_{lf}} \tag{1}$$

where, C is the total output capacitances of two transistors in the same leg and n transformer ratio.

For the transistors S_2 and S_4 ZVS is provided by the resonance between L_{lk} and the transistor output capacitance. The needed energy for achieving ZVS is given as:

$$E = \frac{L_{lk} \cdot I_2^2}{2} \geq \frac{4}{3} \cdot C_{out} \cdot V_S^2 + \frac{C_{TR} \cdot V_S^2}{2} \tag{2}$$

where, I_2 is the primary current when the switch S_2 turn off, V_S is the input voltage, C_{TR} is the transformer winding capacitance (Ma *et al*., 2004). To achieve ZVS for S_2 and S_4 the load current must exceed the critical value.

$$I_{CRIT} = \sqrt{\frac{2}{L_{lk}} \cdot \left(\frac{4}{3} C_{out} \cdot V_S^2 + \frac{1}{2} C_{TR} \cdot V_S^2 \right)} \tag{3}$$

The ZVS for S_1 and S_3 can be achieved even at light loads because D_1 and D_3 can always be turned on by the energy stored in the output filter inductance.

The maximum duty cycle of the converter is shown in Fig. 2 and it can be expressed as (Cho *et al*., 1996):

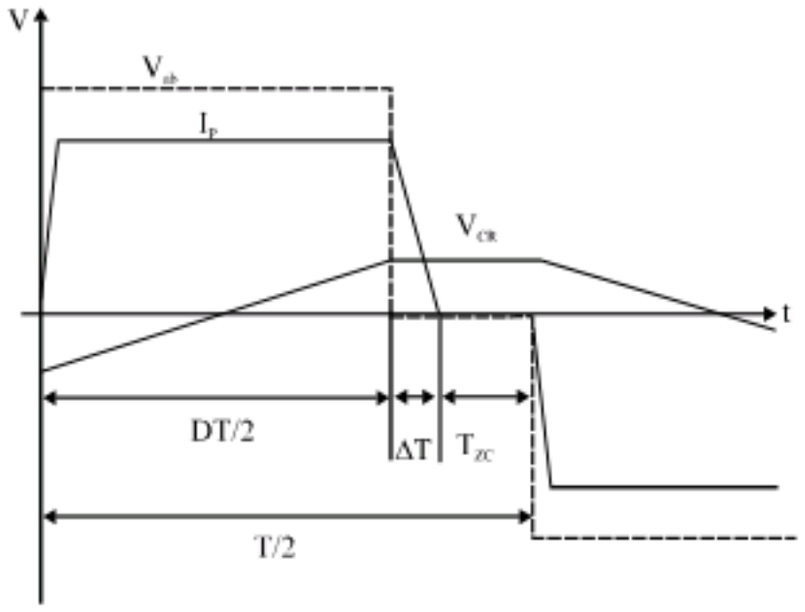

Fig. 2: The duty cycle limit of the converter

$$D_{max} = 1 - \frac{\Delta T + T_{ZC\ min}}{T/2} \quad (4)$$

where, T_{ZC} is the time of mode 4 and 5 where, the primary current I_p is zero. If the blocking capacitor is large enough to be treated as voltage source ΔT can be expressed below:

$$\Delta T = \frac{n I_{ff} DT}{V_{CRP}} \quad (5)$$

where, V_{CRP} is the peak voltage of the blocking capacitor:

$$V_{CRP} = \frac{n I_{ff} DT}{4C} \quad (6)$$

DC-DC converter implementation: A SIMULINK model is constructed from blocks of the C2000 Embedded target Library which are used to represent algorithms and peripherals specific to the C2800 DSP family. A target preference block has to be added to the model, in this case the F2808 eZdsp block. It is not connected to any other blocks, but stands alone to set the target preferences for the model. However, it allows control build options for the compiler, assembler and linker which will be invoked to generate the executable image file for download to the DSP Texas Instruments (2004).

The main part needed to perform the algorithm is the enhanced Pulse Width Modulator (ePWM) module. Two ePWM blocks are used to configure the PWM needed for DC-DC converter. One of the ePWM configured with the duty ratio signal is fixed for S_1 and S_2 and the other two switches S_3 and S_4 controlled through the PID controller. The duty cycle for both of the switching signals is set to be 50%. The change of the output voltage, obtained by the overlap of the switching signal S_1 and S_3 with S_2 and S_4.

The carrier frequency is calculated from the following equations, when the counter setting is up/down:

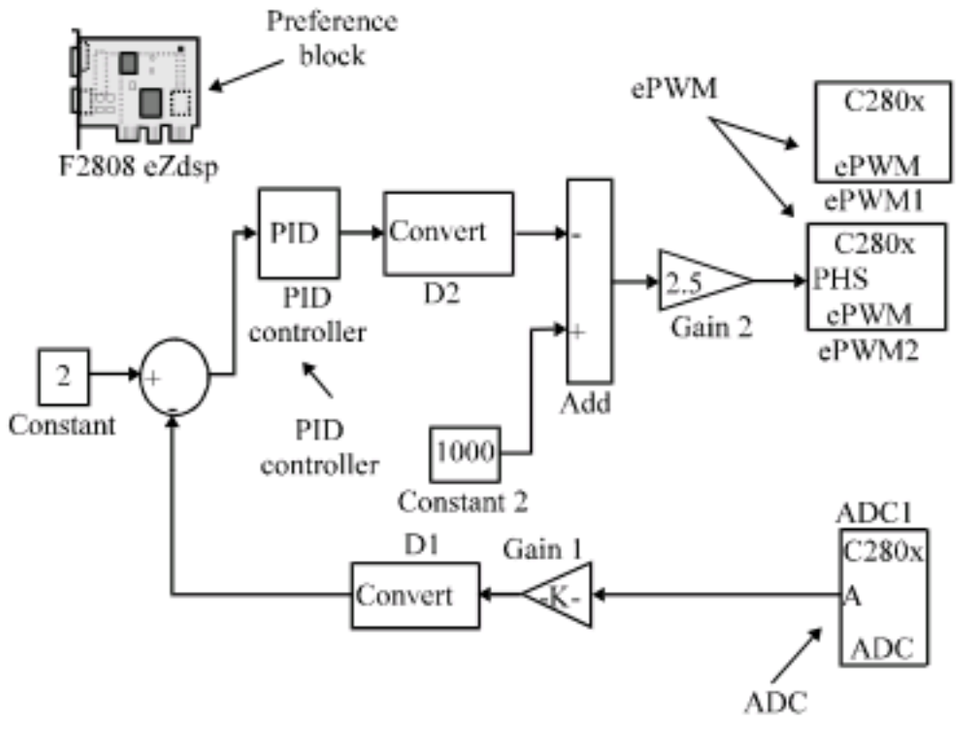

Fig. 3: SIMULINK model for phase-shift PWM

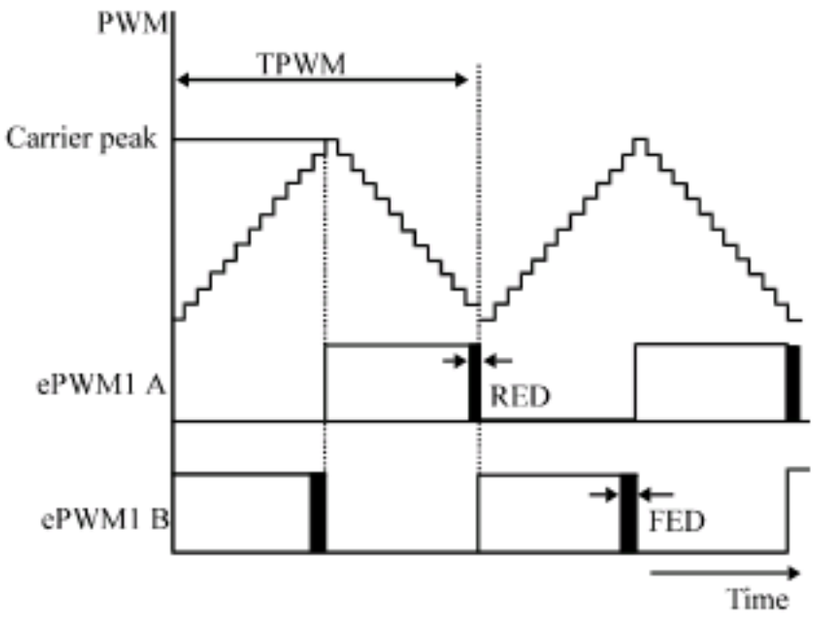

Fig. 4: Generation on PWM using ePWM, with dead band

$$TPWM = 2(TBPRD \times TTBCLK) \quad (7)$$

$$FPWM = \frac{1}{TPWM} \quad (8)$$

$$TBCLK = \frac{SYSCLKOUT}{HSPCLKDIV \times CLKDIV} \quad (9)$$

where, TPWM is the PWM interval, TBRD is the value saved in the TBPRD register, TTBCLK is the time of one clock cycle and FPWM is the carrier frequency. The SIMULINK model for phase shift PWM generation is shown in Fig. 3 and the PWM cycle (TPWM) is shown in Fig. 4.

The dead time is strongly needed to allow the discharge of the switches shunted capacitors. To create dead-time for the switches on the same leg, the Dead-Band (DB) module is used. The DB module supports independent values for Rising-Edge Delays (RED) and Falling-Edge Delays (FED). Equation 10 and 11 are used to calculate FED and RED, respectively (Texas Instruments, 2004):

$$FED = DBFED \times TTBCLK \quad (10)$$

$$RED = DBRED \times TTBCLK \quad (11)$$

PARALLEL INVERTERS

Parallel operation of inverters is a viable way to expand power capacity and achieve N+1 redundancy in power electronics. Each parallel module takes its share of load, so the current stress on power switch is reduced greatly (Lee *et al*., 1998). Higher reliability, larger power capacity, lower cost and the shorter development cycle can be achieved and system configuration becomes flexible by using parallel inverter modules. However, the circulation current between parallel modules results in damage of power semiconductors in the parallel inverter (Ogasawara *et al*., 1992). In order to reduce the effect of circulation current, the output voltage of all paralleled inverters must be strictly consistent in frequency, phase and amplitude to guarantee the output power sharing. In parallel operation, two or more inverters can be tied together to share a load. In this study, a system of two units is discussed for simplicity. The proposed parallel connected inverter is shown in Fig. 5. It consists of two units of standard three-phase inverters. The two inverters are connected directly at the input and through resistors at the output ends of the inverters.

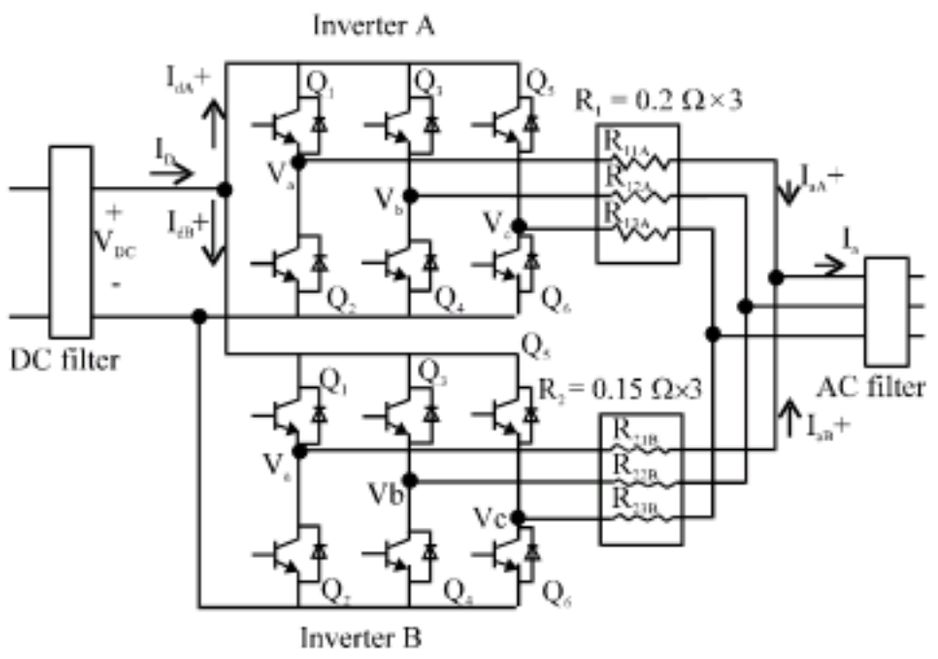

Fig. 5: The proposed connection three-phase inverters in parallel

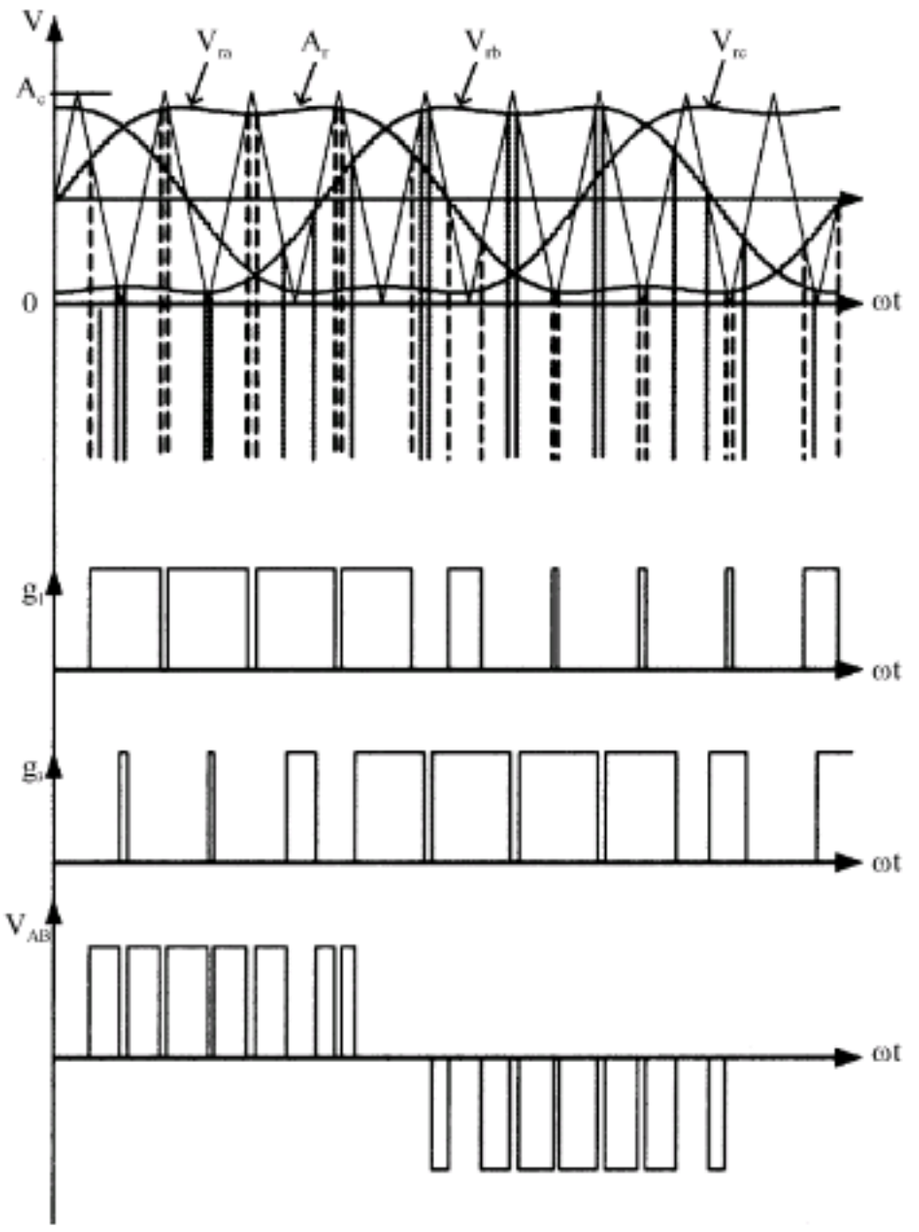

Fig. 6: Generation of THIPWM

Third harmonic injection PWM: Third harmonic injection PWM (THIPWM) is preferred in three-phase application, because third-harmonic component will not be introduced in three-phase systems. THIPWM is better in utilization of DC source (Rashid, 2004). Among the modulation techniques used for three phase inverter, Space Vector Modulation (SVM) extends the linear modulation range 15% more compared with pure sine-wave (SPWM). This advantage can be achieved through injection of triple harmonics to the sine-wave modulating signal which result in third harmonic injection modulation or multiple harmonic injection modulation. The simple and direct implementation of THIPWM gives it advantage over the SVM, for the reason that no needs to track the operating sector or add a state machine for switch sequencing of THIPWM. In terms of harmonic distortion, high switching frequency THIPWM makes it appropriate for harmonic distortion elimination (Kwasinski *et al*., 2003). The generation of THIPWM is shown in Fig. 6. Figure 7 shows the over all control design of the three-phase inverter. In THIPWM, the modulating signal is compared with the triangle signal which was provided by enhanced Pulse Width Modulator (ePWM). The data stored in the look-up table for phase a, b and c is calculated using the following equations:

$$V_{ra} = 1.15\sin\omega t + 0.19\sin 3\omega t \quad (12)$$

$$V_{rb} = 1.15\sin\left(\omega t - \frac{2}{3}\pi\right) + 0.19\sin 3\omega t \quad (13)$$

$$V_{rc} = 1.15\sin\left(\omega t - \frac{4}{3}\pi\right) + 0.19\sin 3\omega t \quad (14)$$

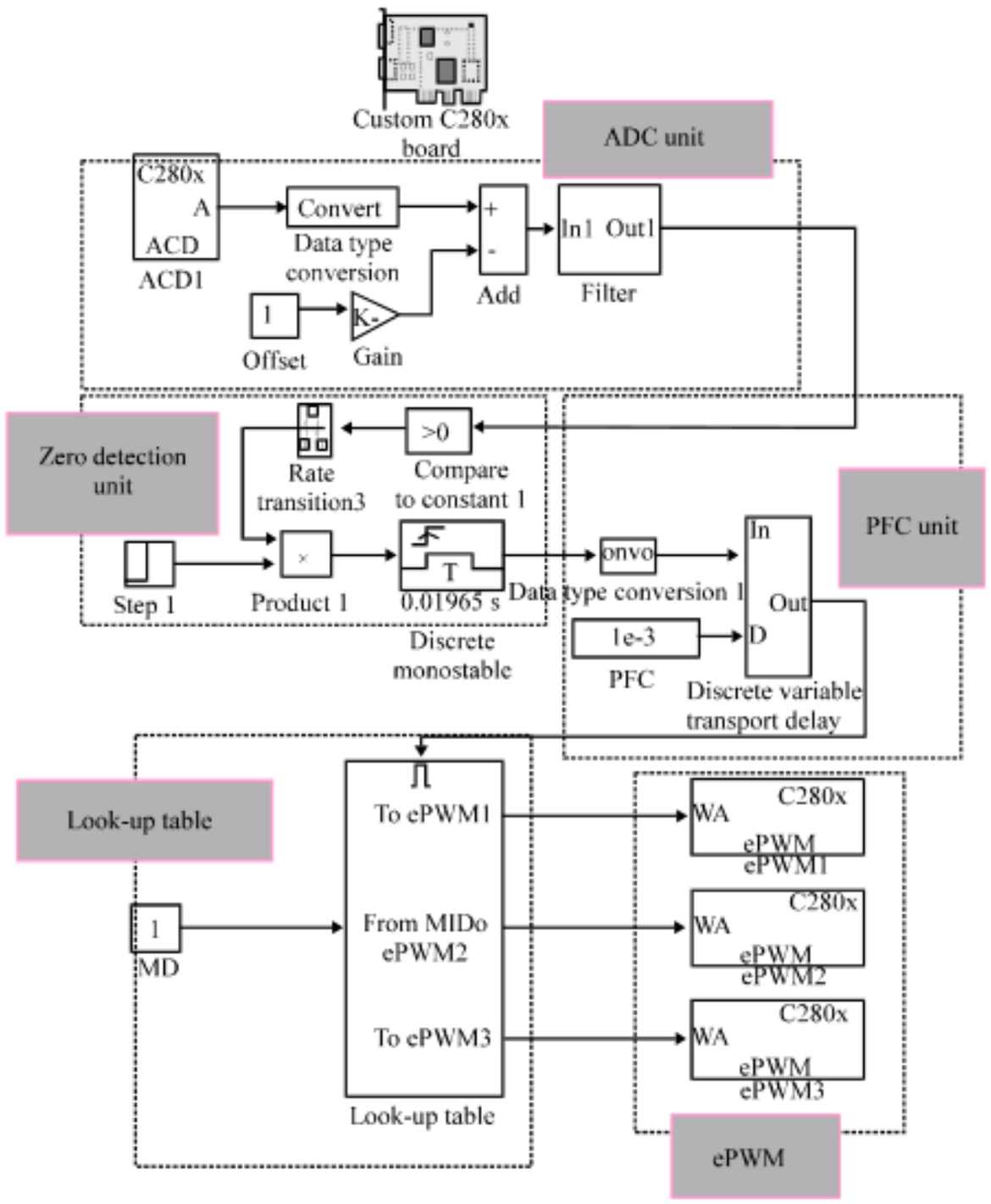

Fig. 7: Control design of the three-phase inverter

The modulation index control is accomplished by using multiplier units that multiply the external data with the stored data in the look-up tables. The multiplying block produces outputs using either element-wise or matrix multiplication, depending on the value of the multiplication parameter. Offset value added to each phase data to shift the phase data higher than zero to be compared with the carrier signal, which generated by using Up-down counter.

Switching cycle: In the generation of THIPWM, some elements need to be considered in order to get accurate switching signal suitable for three-phase inverter. The elements are zero detection unit, Power Factor Correction (PFC) unit and Dead Band (DB).

Software implementations of zero detection unit to replace phase locked loop were investigated to avoid building additional hardware for the phase locked loop. The zero detection unit used to obtain no phase shift between the inverter output voltage and the grid voltage. A comparator is used to compare the filtered signal with positive zero. The comparator block detects the positive

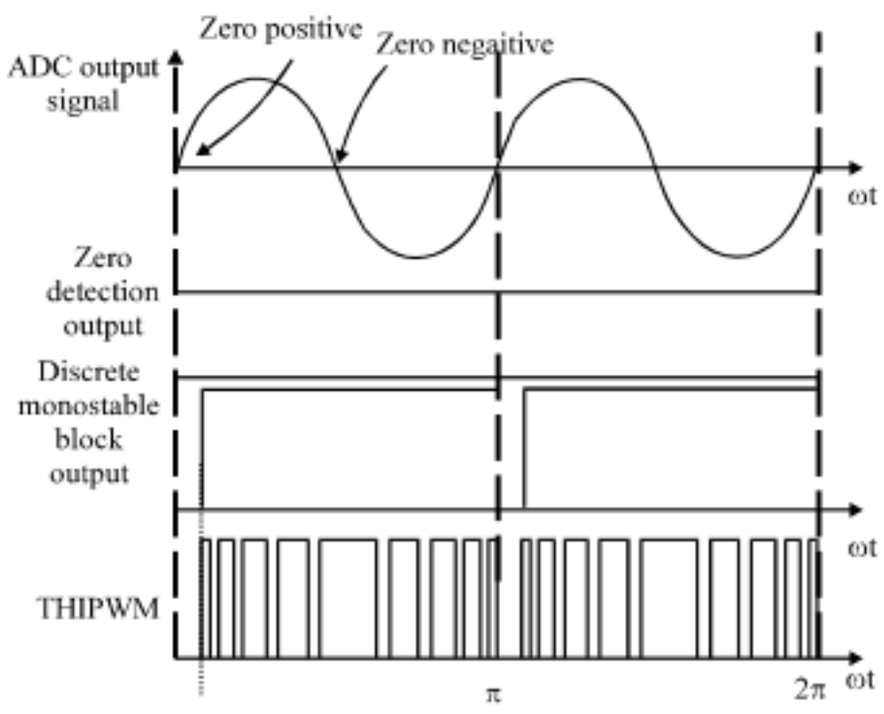

Fig. 8: Zero detection for voltage synchronization

zero and produces a logic high-signal on its output as shown in Fig. 8. This signal will trigger the lock-up table sub-system by adding an enable block to a subsystem. An enabled subsystem executes when the input received at the enable port is greater than zero. To get the signal

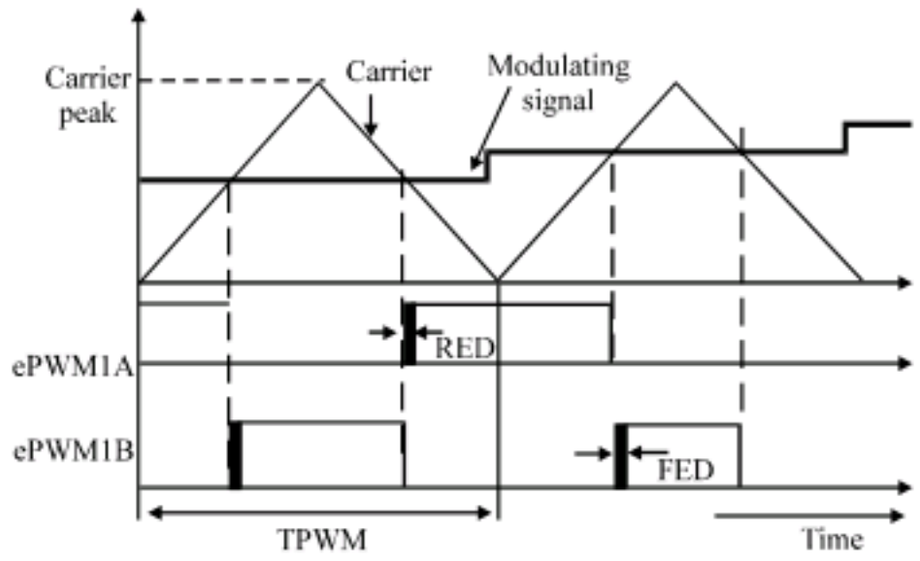

Fig. 9: THIPWM switching cycle

suitable to the trigger block with high and low properties, discrete monostable block is used. The output of the discrete monostable block is a square pulse with 50 Hz frequency and a duty cycle of 98%. The discrete monostable block produces trigger-signal to trigger the look-up table sub-system, result in the THIPWM generation being locked to the grid voltage. The starting point of the PWM is obtained using discrete variable transport delay block. Both zero detection unit and PFC units are interacting together to obtain the right starting point of the THIPWM signal. This will allow the inverter output voltage to be in phase with the grid voltage and the inverter voltage and the current are in phase. To prevent a short circuit in the DC link of IGBT voltage source PWM converters, when the upper and lower IGBTs of the same leg are off, dead time period need to be inserted in switching signals (Zhang *et al*., 2005). Right selection for the dead time value avoids a waveform distortion and the fundamental voltage loss. Figure 9 shows the THIPWM switching cycle.

Current sharing and circulating current: Inverters with different ratings are some times connected in parallel especially for system upgrading or to enhance the power rating of any used inverter. In this case, it is desirable for the paralleled converters to share the currents equally. If the inverter uses non-identical IGBT's, current sharing and circulating current are considered. To study the current sharing and circulating current, Fig. 10 shows one mode of operation, where the current I_{dA}^{+} flowing through Q_{1A} and Q_{1B}. However the current I_{dA}^{-} flows back to the source through Q_{6A} and Q_{6b}. The current is sharing between Q_{1A} and Q_{1B}, with the addition of two series resistors.

Current sharing depends on the IGBTs Q_{1A} and Q_{1B}. If V_{CE1A} is not equal to V_{CE1B}, I_{dA}^{+} will not be equal to I_{dB}^{+}. To maintain similar current sharing between the two inverters, series resistors R_1 and R_2 are added between

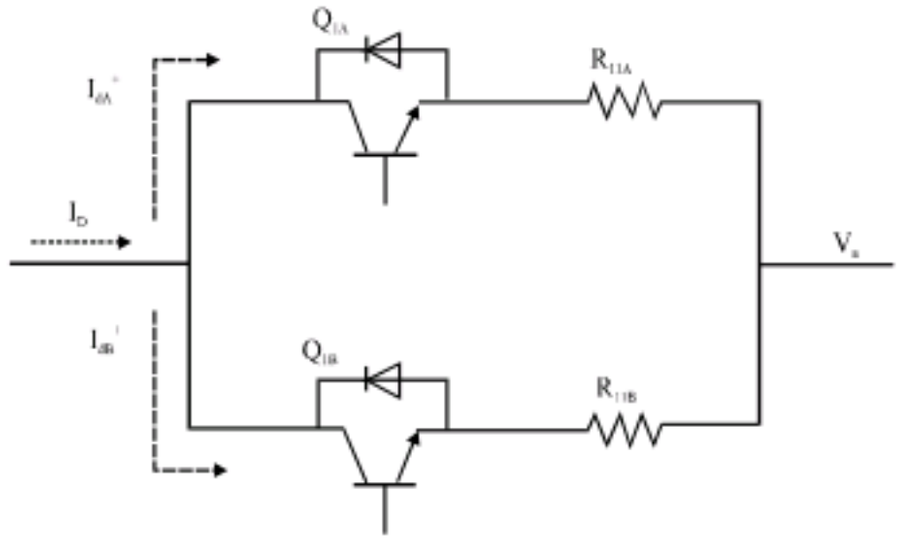

Fig. 10: Current path during one switching cycle

each of the six legs and the common point R_1 box consists of three resistors, R_{11A}, R_{12A} and R_{13A}. Similarly R_2 consists of R_{21B}, R_{22B} and R_{23B}. Adding the resistances R_{11A} and R_{11B} suppose to satisfy the following condition:

$$V_{CE1A} + I_{dA}^{+} \cdot R_{11A} = V_{CE1B} + I_{dB}^{+} \cdot R_{11B} \tag{15}$$

Assuming that:

$$I_{dA}^{+} = I_{dB}^{+} = \frac{I_D}{2} \tag{16}$$

$$\frac{I_D}{2}(R_{11A} - R_{11B}) = V_{CE1B} - V_{CE1A} \tag{17}$$

or

$$R_{11A} = \frac{2(V_{CE1B} - V_{CE1A})}{I_D} + R_{11B} \tag{18}$$

For the correct value of R_1 and R_2, each of them should be much smaller than the load resistance. The circuit will experience similar current sharing in all the modes of operation as a result the circulating current will be small. The DC current flow to each inverter is half of the total DC- current:

$$I_{dA}^{+} = I_{dB}^{+} \cong \frac{I_D}{2} \tag{19}$$

At the AC-side, the two inverter currents are united back to the AC load through a common LC filter.

$$I_{aA}^{+} + I_{aB}^{+} = I_a,\ I_{aA}^{+} \cong I_{aB}^{+} \text{ and } I_a \cong 2I_{aA}^{+}$$

GRID CONNECTED SYSTEM

The DC voltage produced by the DC power supply is converted to a high-frequency train of positive and

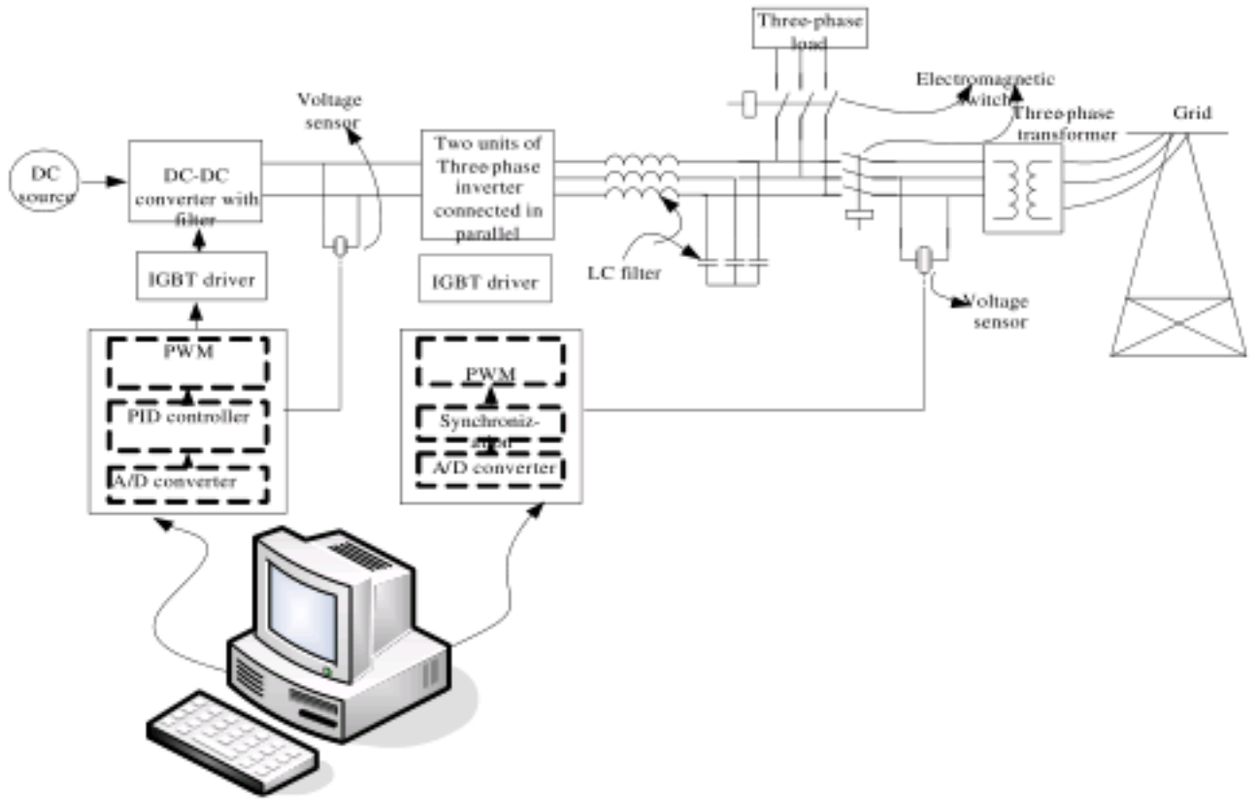

Fig. 11: Full system setup including grid connection

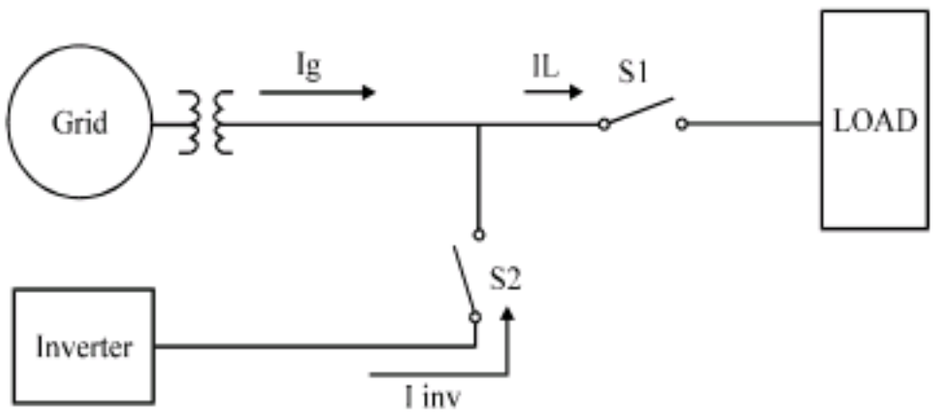

Fig. 12: System connection to the grid

negative pulse pairs by the full-bridge converter, which is controlled by the phase-shift modulation technique. The high-frequency transformer isolates the DC source from the grid and steps up the amplitudes of the pulses to the level required for successful control of the grid voltage. The DC-DC converter supplies a power to three-phase parallel-connected inverter. The six-step modulation uses a sequence of six switch patterns for three-phase full-bridge inverter, to generate a full cycle of three-phase voltages. The inverter output voltage has the same frequency and amplitude with those of the grid voltage. Figure 11 shows the full system setup including the grid connection. The proposed system is connected to the grid through transformer to provide isolation and to step-up the voltage to the required level. The proposed system is designed to supply the three-phase load and the grid as well. The simplified connection arrangement presented in the single line diagram is shown in Fig. 12. The electromagnetic switch S_1 connects the power to three phase load from the grid and the inverter. The electromagnetic switch S_2 connects the inverter to the grid.

RESULTS AND DISCUSSION

A prototype model of the grid connected system was constructed and tested to verify the proposed system's operation. The prototype hardware design has been discussed in earlier. Here, experimental result with closed-loop system is presented. Parallel connected three-phase inverter and the grid connected system are also presented. The parameters of the system are selected as shown in Table 1. The connection of two parallel inverters with different IGBT ratings and without the balance resistors R_1 and R_2 connection produces unbalanced currents at the output of each inverter, as shown in Fig. 13. However, after the resistor connection for the same IGBT configuration, the currents at the two inverter outputs were approximately balanced and they are shown in Fig. 14. The phase current peak in inverter A, $I_{Aa\ Peak} \approx 2$ A and the phase current peak in inverter B, $I_{ba\ Peak} \approx 2.7$ A. By adding the balance resistors to the parallel connected inverters the phase current peak in inverter A $I_{aa\ Peak} \approx 2.4$ A and the phase current peak in inverter B $I_{Ba} \approx 2.4$ A. The similar current in each inverter side minimizing the circulating current in between the inverters. The value of the resistors used was 0.15 and 0.2 Ω unlike the impedance value used by Cai *et al*. (2008). The low resistor value reduces the power dissipation on the resistors which improve the inverter efficiency. The results obtained in the proposed system are the same as what have been reported in literature in term of current balance in the parallel inverters. The proposed parallel inverter in this study experience higher efficiency due to the low resistor value used, that's shown in Table 2. The use of DSP allows accurate control of the THIPWM switching signal which allows the control

Table 1: System components and parameters

Three-phase inverter	IGBT for inverter A is SSG60N60 $V_{CE(oN)}$=1.75 V
	IGBT for inverter B is IRGP50B60PD1 $V_{CE\ (oN)}$ = 2 V
	LC at grid side L = 1 mH C = 5 μF
	Carrier frequency = 4.5 kHz
	R1 = 0.2 Ω
	R2 = 0.15 Ω
	Modulation index = 0.95
DC/DC converter	IGBT SSG60N60 with $V_{CE(oN)}$ = 1.75 V
	Filter C = 220 μF
	Carrier frequency = 20 kHz
PID values	Kp = 9.6, Ki = 96000, Kd = 0.0024
H/F transformer	Core: SF-40 EE core from new favour industry
	Primary turns: 9 turns
	Secondary turns: 45 turns
DSP board	TMS320F2808

Table 2: Compare parallel-connected inverters with single inverter in term of input and output power, current THD and voltage THD

Inverter	I_{DC} (amp)	V_{DC} (V)	Input power (W)	I_P (amp)	V_P (V)	Output power (W)	Efficiency (%)	Current THD (%)	Voltage THD (%)
Single	3.72	250	930	3.07	98.7	909	97.7	1.42	1.43
Double	3.78	250	945	3.10	100	930	98.4	1.36	1.28

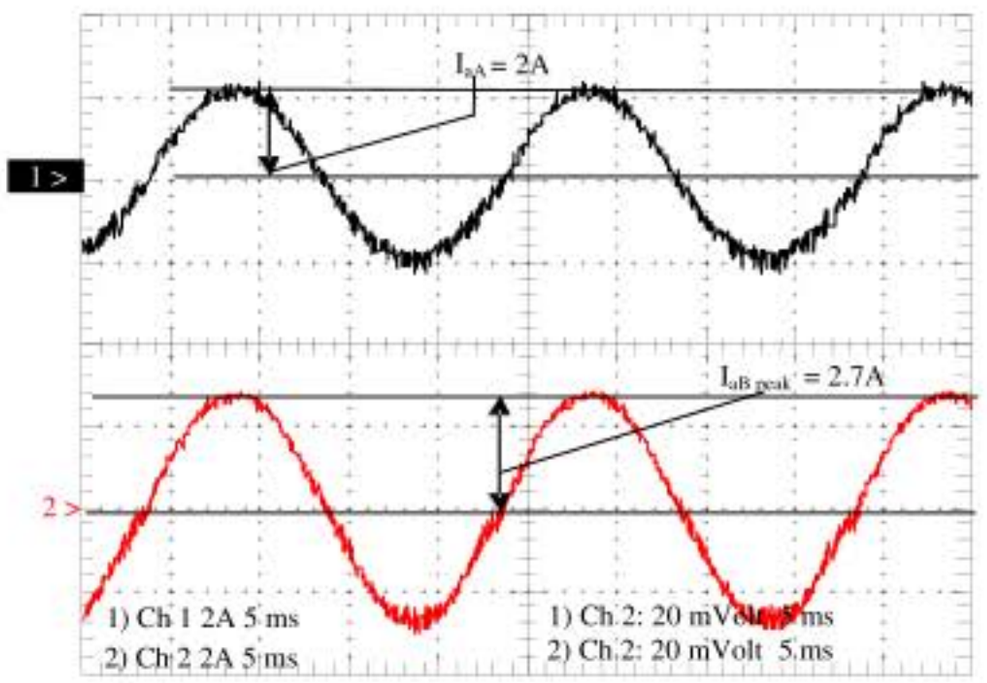

Fig. 13: Current at each inverter output without resistor connection (2 A/div, 5 m sec/div)

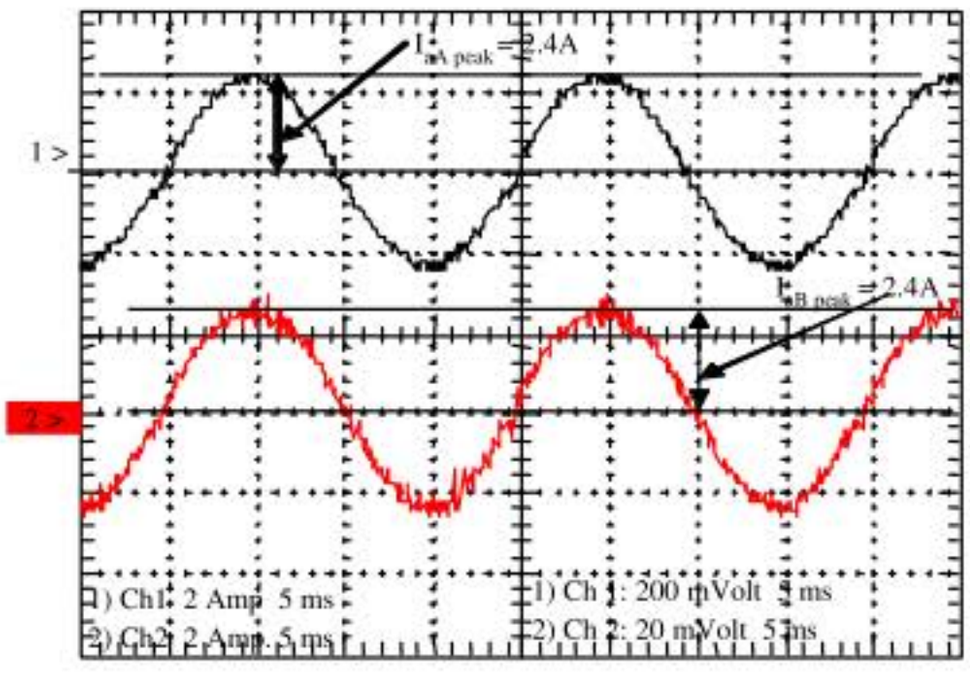

Fig. 14: Current at each inverter output with resistor connection (2 A/div, 5 m sec/div)

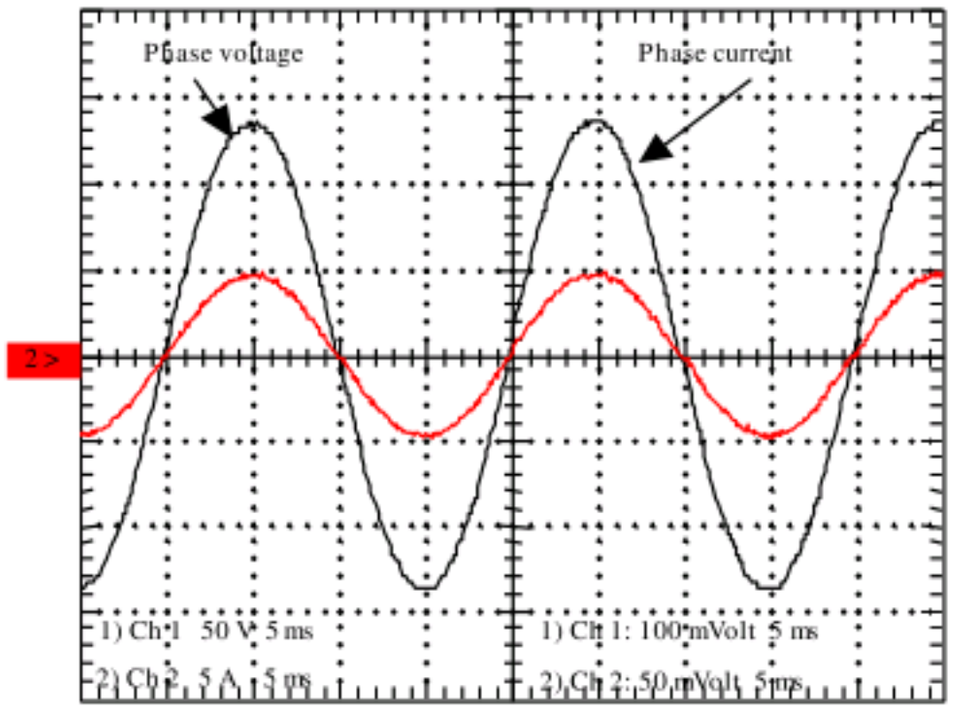

Fig. 15: Phase voltage and phase current on the load side (50 V/div, 5 A/div, 5 m sec/div)

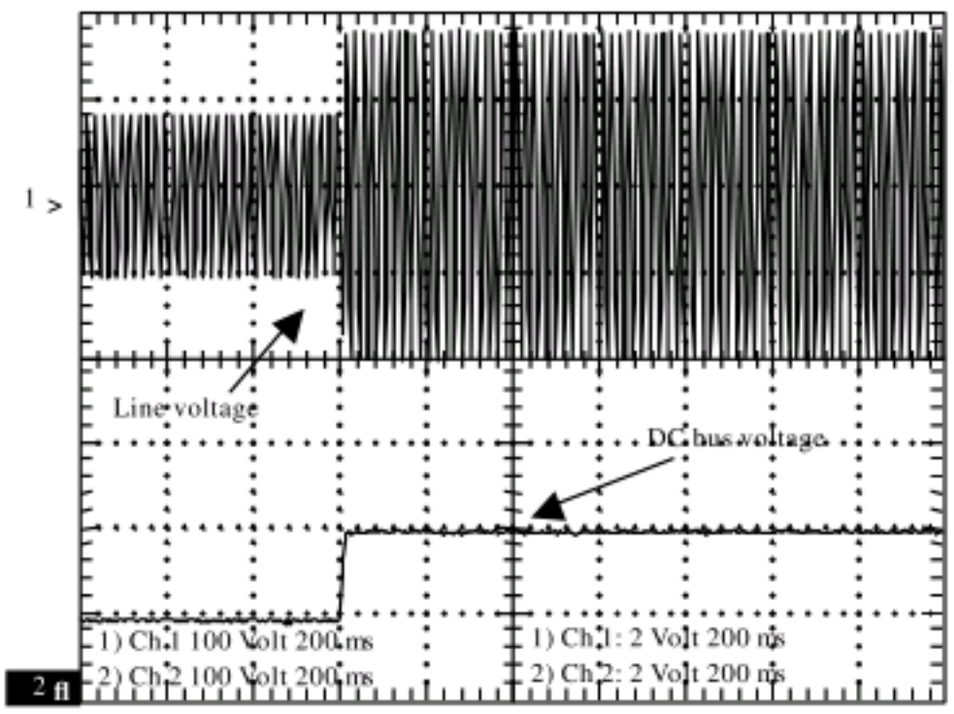

Fig. 16: Step response for DC signal and AC signal (100 V/div, 100 V/div and 200 m sec/div)

of the voltage current phase-shift. The control algorithm implemented in such way that the drown current is in phase with the phase voltage of the inverter. The phase voltage and current are in phase as shown Fig. 15. Closed loop test has been carried out for the three-phase balance with inductive load. Figure 16 shows the AC and DC step change from 100 to 200 V, respectively. It is clearly shown that the change of DC voltage from 100 to 200 V took a settling time of less than 20 msec. To connect the inverter to grid the voltages of both sides must be in phase and the inverter voltage suppose to be higher than the grid voltage to allow the power flow to the grid. The grid voltage and the inverter's output voltage before and after the grid connection is shown in Fig. 17 the voltages are in phase and the inverter voltage is slightly higher than the grid voltage. To prove that the system is feeding power to the grid switches S_1 and S_2 kept closed, which makes both the inverter and the grid contribute currents I_{inv} and I_g to the load as shown in Fig. 18 after S_1 opens, all the current produced by the inverter will feed the grid as Fig. 19 shows the grid's phase-voltage (V_g) and the phase current (I_L). Table 2 shows a comparison between single inverter and parallel connected inverter. The results presented in this study shows better THD and efficiency in the three-phase inverter compared by Cai *et al*. (2008). That's due to the accurate generation of THIPWM and the low resistor value used compared by Naik *et al*. (1995) and Cai *et al*. (2008). The result shows the validity of the distributed generation system with parallel connected inverter. And it validates the parallel connected inverter operation in term of efficiency and the THD. If the proposed systems compared with the systems given by Vázquez *et al*. (2008) it will be easily found that it obtains better THD and efficiency.

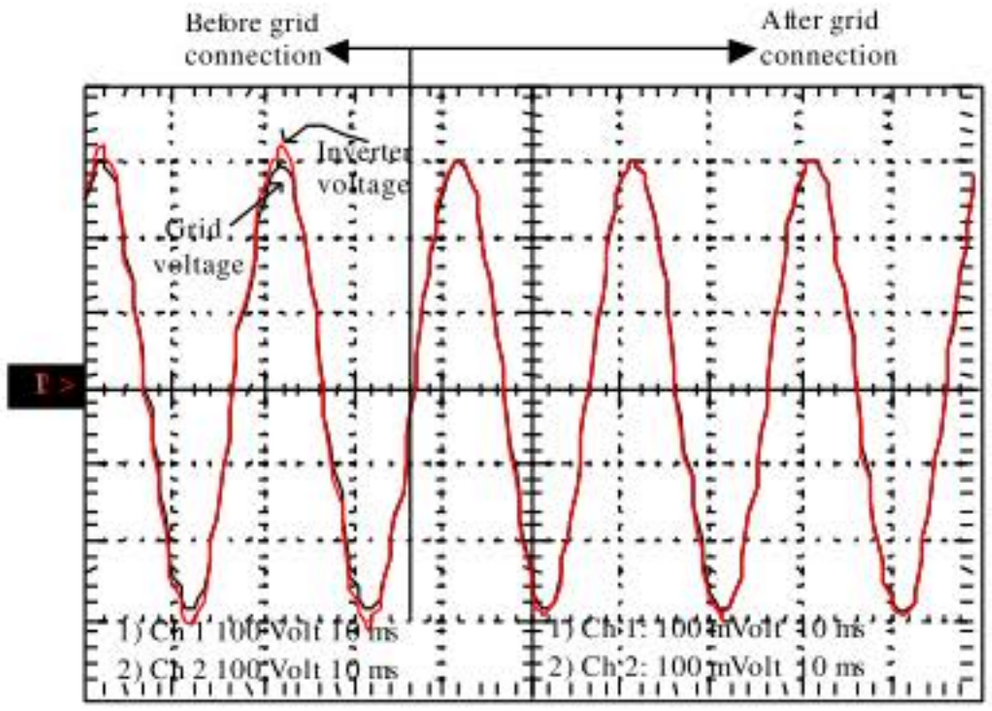

Fig. 17: Line voltage on the grid and the inverter output (100 V/div, 10 m sec/div)

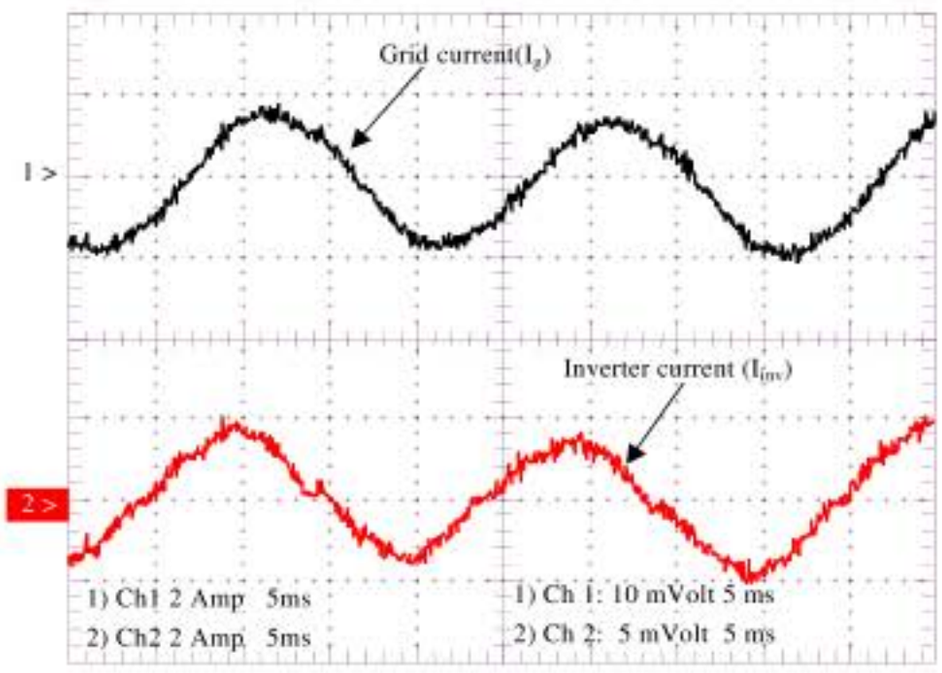

Fig. 18: Grid current and the inverter current feeding the load (2 A/div, 5 m sec/div)

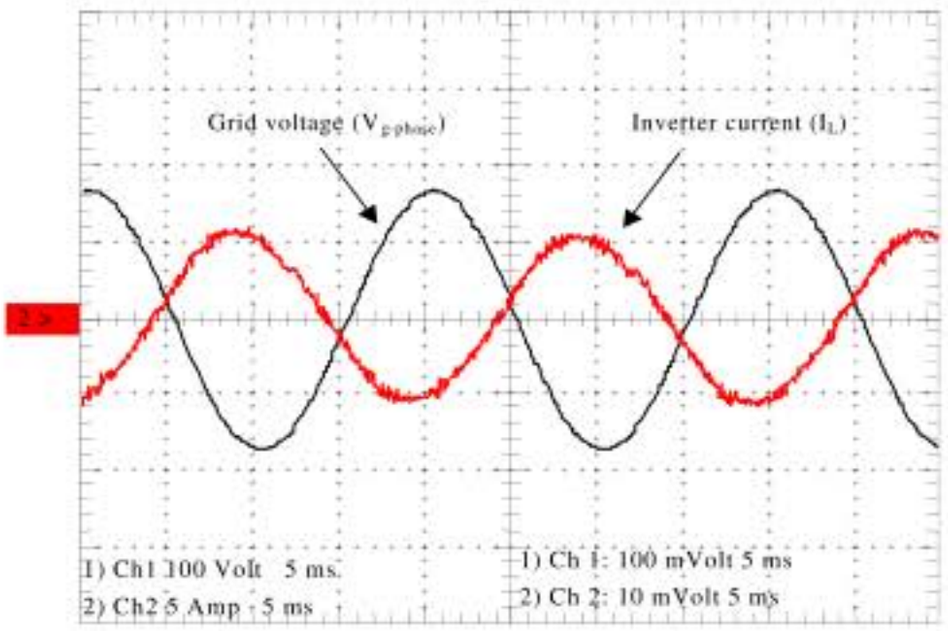

Fig. 19: Grid phase voltage and the current feeding the grid (100 V/div, 5 A/div, 5 m sec/div)

CONCLUSION

The inverter performance was satisfactory in terms of reducing the current and voltage Total Harmonic Distortion (THD) injected to the grid. From the experimental result, it shows that the THD of the inverter output current and voltage injected to the grid are within the stipulated limits laid down by the

international standard. The improvement of parallel connection over single inverter is shown in terms of improvements in THD and inverter efficiency. The two inverters shared the same current value that allows circulating current to be minimum. By selecting the right passive filter, low balance resistor value and the suitable IGBT, parallel connected inverter could operate with high efficiency.

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