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Leakage Tolerant, Noise Immune Domino Logic for Circuit Design in the Ultra Deep Submicron CMOS Technology for High Fan-in Gates

[1]A. Peiravi, [2]F. Moradi and [2]Dag T. Wisland
[1]Department of Electrical Engineering,
School of Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
[2]Nanoelectronics Research Group, Department of Informatics, University of Oslo, NO-0316 Osolo, Norway

Abstract: In this study, the results of research carried out in order to develop and present a new logic for the design and development of leakage-tolerant and noise immune circuits in the ultra deep submicron CMOS technology are presented. We present novel domino logic to overcome the increasing static power consumption due to leakage power and to improve noise-immunity for high fan-in gates and compare it with standard domino logic. A noise metric and ISO-delay conditions are used to compare present proposed logic with conventional domino logic for various high fan-in OR gates. The results show remarkable improvement in noise immunity while drastically reducing power consumption.

Key words: Leakage tolerant, noise-immune, ultra deep submicron CMOS technology, domino logic, high fan-in gates

INTRODUCTION

The high speed characteristics of domino circuits are primarily due to their low noise margin. Ding and Mazumder (2004) argue that dynamic CMOS gates are inherently less resistant to noises than static CMOS gates and present noise-tolerant design technique using circuitry exhibiting a negative differential resistance effect. Ding and Mazumder (2004) presented results using a supply voltage of 1.6 V and showed that the input noise immunity level can be increased to 0.8 V for about 10% delay overhead and to 1.0 V for only about 20% delay overhead. However, the low noise margin increases the sensitivity of domino logic circuits to noise. As the noise margin of domino logic increases with the down-scaling of the manufacturing technology and the increasing of their operational frequency, the error-free operation of domino logic circuits is the most important challenge. The decreased threshold voltage with scaling down the voltage supply increases the speed while it places the power consumption at an acceptable level. However, the decreased threshold voltage decreases the noise immunity because of the increasing sub-threshold leakage current.

Sub-threshold leakage current increases exponentially with scaling down of the manufacturing technology especially for Ultra Deep Submicron (UDSM) CMOS technology and the increase in temperature. The dynamic power due to scaling supply voltage is controlled, but the static power is increased with the technology scaling if we only scale down the threshold voltage of devices. We also have to scale down the threshold voltage; otherwise, the delay will increase significantly. Kim and Roy (2001) presented a leakage tolerant dynamic circuit called Source Following Evaluation Gate (SFEG) which has high DC noise margin. They presented simulation results in 0.13 and 0.1 μm CMOS process technologies and showed considerable degradation in noise immunity of domino circuits with threshold voltage scaling and/or increase of fan-in. Their comparison with standard domino circuits showed the noise immunity of 16-input OR SFEG is 37% higher than domino circuit with same delay and that the noise characteristic of SFEG is insensitive to fan-in and hence, the difference of noise immunity between SFEG and domino becomes larger with the increase in fan-in. Elgamel *et al.* (2003) proposed a low voltage noise tolerant XOR-XNOR gate with 8 transistors which was implanted in an already existing (5-2) compressor cell to test its driving capability. They used the average noise threshold energy (ANTE) and the energy normalized ANTE metrics to quantify the noise immunity and energy efficiency, respectively in 0.18 m CMOS technology. They showed that the proposed XOR-XNOR circuit was more noise-immune with a better power-delay product characteristics than existing circuits and worked at all ranges of supply

Corresponding Author: Ali Peiravi, Department of Electrical Engineering, Faculty of Engineering, Ferdowsi University of Mashhad, Postal Code 9177948974, Mashhad, Iran
Tel: 098-0511-881-5100/653 Fax: 8763302

voltage starting from 0.6 to 3.3 V. Baozeng *et al.* (2006) presented two new circuit techniques to suppress leakage currents and enhance noise immunity while decreasing the active power. They used 8-input OR gates and showed that the proposed circuits effectively lowered the active power, reduce the total leakage current and enhance speed under similar noise immunity conditions. The active power of the two proposed circuits was reduced by up to 818 and 1118% while enhancing the speed by 915 and 1317% as compared with dual V_t domino OR gates with no gating stage.

Domino logic circuit techniques are widely used compared with CMOS static circuits due to their high performance and area characteristics. Moradi *et al.* (2004, 2005) presented a new domino circuit for high fan-in and high-speed applications in ultra deep submicron technologies. Their proposed circuit employs a footer transistor that is initially OFF in the evaluation phase to reduce leakage and then turned ON to complete the evaluation. According to simulations in a predictive 70 nm process, their proposed circuit increases noise immunity by more than 26X for wide OR gates. They showed a performance improvement of up to 20% compared to conventional domino logic circuits. Cheng (2008) presented a domino circuit with a master evaluation node to which a master discharge path with a wide input and gate is couple and a virtual evaluation node to which output stage and slave discharge paths are coupled.

SCALING AND LEAKAGE CURRENT

Consider Fig. 1 in which we show a single NMOS transistor whose source is grounded. The drain to source current vs. the drain to source voltage as VGS is varied for different temperatures for this transistor is shown in Fig. 2.

You can see the effect of the drain voltage on the leakage current as shown in the following equation:

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right)$$

Where:

$$I_{ds0} = \beta v_T^{\ 2} e^{1.8}$$

and the thermal voltage $v_T = KT/q$ and n is defined as follows:

$$n = 1 + \frac{C_{dm}}{C_{ox}}$$

with C_{dm} as the depletion layer capacitance and C_{ox} as the oxide capacitance. We can see the current scaling trends

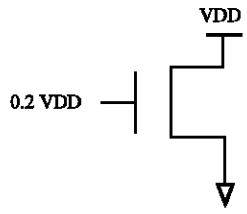

Fig. 1: A grounded NMOS transistor

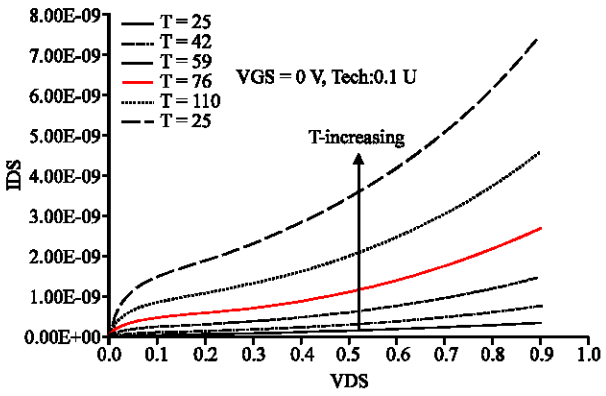

Fig. 2: The drain to source current vs. the drain to source voltage as the gate-to-source voltage V_{GS} is varied for different temperatures

in the microelectronics manufacturing industry towards ultra deep submicron region would lead to serious reduction in the gate oxide thickness, an increase in C_{ox} and a drastic increase in leakage current.

NOISE METRIC

Unity Noise Gain (UNG) define as the noise metric for present simulations and define it as the amount of noise required for the output voltage to equal the input voltage while we vary noise. This is simulated by applying square waves of amplitude of 0.2 V to present inputs in the n-input OR gate with the width of 30 ps.

$$UNG = \{X_{noise}, [V_{out} = V_{in}]\}$$

The effect of temperature variations on leakage current as a function of gate to source voltage is shown in Fig. 3, where we have applied a square wave of amplitude 0.2 VDD and width of 30 ps to the gate of the transistor and used 70 nm CMOS technology. You can see the increase in the leakage current.

If we could apply a dc voltage to the source of the NMOS transistor in its static conditions, we can increase its threshold voltage and considerably reduce its static leakage current. As there will also be a reduction in the

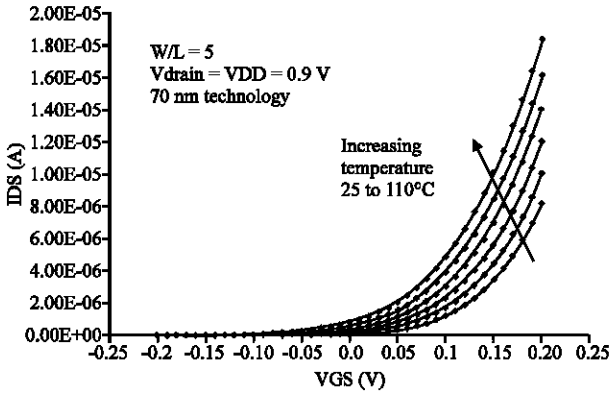

Fig. 3: The effect of temperature on leakage current vs. gate to source voltage

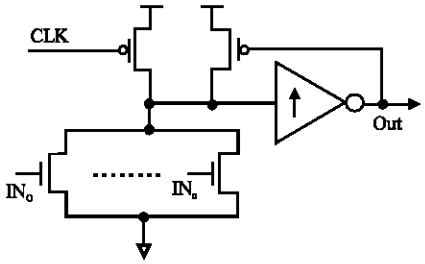

Fig. 4: FLDL domino circuit

operating speed of the circuit, we must find a trade off between leakage current and speed.

STANDARD DOMINO CIRCUITS

Here, we present an analysis of FLDL and Footed Domino Logic (FDL) domino logic circuits due to their importance. We shall present the results of our simulations of high fan-in OR gates due to their importance in high speed applications in the several GHz frequency range. An FLDL circuit is shown in Fig. 4 with n inputs and a keeper transistor to stabilize the state of the output node. When all the inputs are at a low state, the output node should remain as it was before. However, leakage results in a dip in the voltage of the output node which may even get worse due to noise and may lead to an erroneous change of state in the output node as shown in Fig. 5.

One may suggest an increase in the size of the keeper transistor while reducing the size of the evaluation transistors. However, this would lead to more delays in the evaluation phase and also result in the reduction of speed of the circuit. There must be a trade off between circuit speed and noise immunity and leakage tolerance. The leakage current increases as the number of input gates n increases which would lead to a reduction in the noise immunity and leakage tolerance.

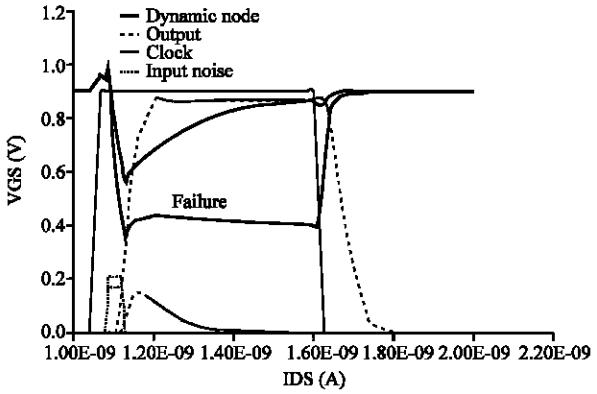

Fig. 5: The dip in the dynamic node due to leakage and input noise showing an erroneous output for 16-in FLDL OR gate (70 nm- 11°C)

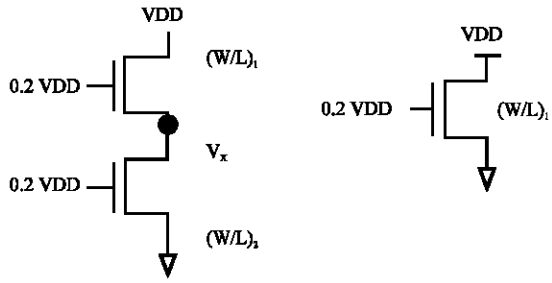

Fig. 6: A single NMOS transistor versus a stacked NMOS transistor pair

The present study propose to use an NMOS transistor in the source side of the evaluation transistors which would help offset the stacking effect.

Now let us consider the FDL circuit. First let us define K as shown in the equation below:

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{Evaluation transistor}}}$$

Noise immunity is improved as this ratio is increased while the speed of operation of the circuit increases as this ratio is decreased. We showed that the waveform of the voltage of the dynamic node would experience a false dip due to the leakage of the parallel transistors in the evaluation leg of the circuit. Consider the stacking effect by looking at the circuit of Fig. 6.

Once we apply 0.2 VDD to the gates of the transistors, there will be a reduction in leakage current in the case of stacked transistors when compared to the single transistor.

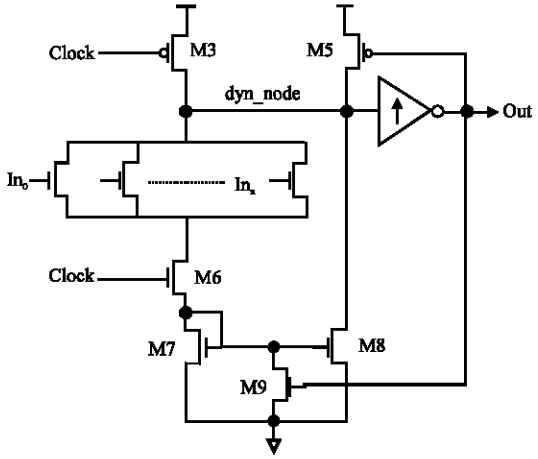

Fig. 7: The proposed circuit with a high level of noise immunity

Present proposed logic: We present this proposed logic in Fig. 7 in which we maintain the voltage of present N-FOOT node at a DC level during static conditions as a result of which we can drastically reduce leakage current. The ratio K is defined as below:

$$K = \frac{(\frac{W}{L})_{M8}}{(\frac{W}{L})_{M7}}$$

A current source is used in present circuit to maintain the output state during static conditions. The circuit works as follows: M3 is on during precharge and the dynamic node shown as dyn_node will charge up to VDD forcing the output voltage to ground and transistor M5 will be turned on. This will expedite the charging of the dynamic node and the precharge process. The gate of the mirror current source that is added here to the standard domino circuit will never reach to the threshold voltage V_{th} of the NMOS transistors of the current source. Thus, there in no power consumption problem in the precharge cycle. The only cause for worry is the leakage current through transistor M8 whose drain is at VDD and a possible small voltage at its gate. The operation of the circuit in the evaluation phase can be divided into two conditions:

- The condition when all applied voltages to the inputs are at ground. This is the static or rest condition of the circuit. There is an exponential reduction in the leakage current due to a negative bulk to source voltage and an increase in the threshold voltage. There is also an exponential decrease in the sub threshold leakage current due to a reduction of gate to source voltage. The resulting waveforms are shown in Fig. 8

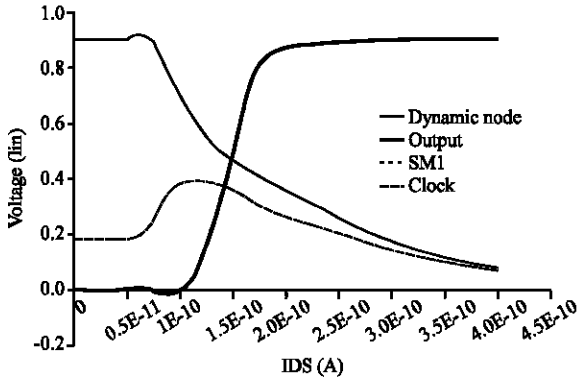

Fig. 8: Waveforms of the various nodes in the proposed circuit

- The condition when any one (or more) of the applied voltages to the input is VDD. In this condition, transistor M6 will turn on just as it does in the rest condition, but the gates of transistors M7 and M8 will start to charge up depending on the number of active inputs on the evaluation circuit. This would slowly result in the discharge of the dynamic node, but the speed of discharge is less than that of the standard domino circuit. Once the output voltage goes beyond the threshold voltage of transistor M9, it will turn off the current mirror and the circuit continues to act like footed Domino logic (FDL)

The gain of present proposed logic is improved noise immunity, reduction in leakage current and an appreciable reduction of static power consumption. The main objective is to present a new logic design for high fan-in circuits with high noise immunity and low leakage power for the ultra deep sub-micron CMOS technology. We have performed present simulations under ISO-delay conditions for all circuits and compared their performance. We have assumed a small size for the keeper transistor in order to control the speed using the mirror transistors thereby reducing the contention between the keeper transistor and the evaluation leg of the circuit. This is how we can achieve a reduction in the dynamic power consumption of the circuit.

SIMULATION RESULTS AND CONCLUSIONS

The simulations were performed at a voltage of 0.9 Volts, 110°C and used HSPICE using low threshold model for NMOS transistors. The results of present simulations are shown in Fig. 9 for various fan-ins from 8 to 64. Here, we have varied the size of the keeper transistor from 0.1 to 1 for the conditional footer logic. We also varied the ratio of the mirror from 0.25 to 1.

Table 1: A comparison of noise metric for standard domino, conditional keeper and our proposed conditional footer domino logic

	UNG (unity noise gain) Comparison under same delay				
Fan-in	UNG of standard domino	UNG of conditional -keeper domino	UNG of proposed domino	UNG improvement compared to standard domino	UNG improvement compared with conditional-keeper domino
8	0.17	0.24	0.345	2.0X	1.4X
16	0.13	0.16	0.480	3.7X	3.0X
32	0.09	0.09	0.490	5.4X	5.4X
64	0.03	0.05	0.530	17.7X	10.6X

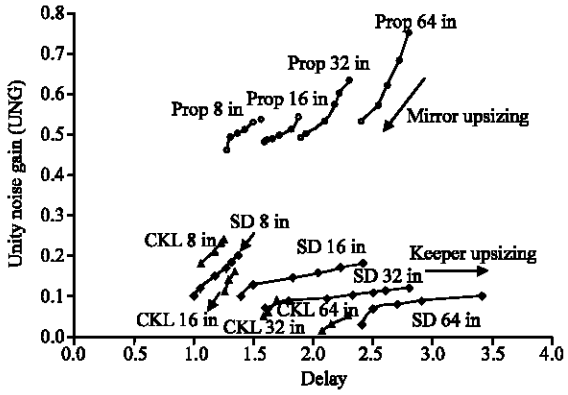

Fig. 9: The comparison of results using UNG metric

A comparison of the results is presented in Table 1 and shown in Fig. 9 where we have compared the behavior of FDL, FLDL and present proposed CFL logic. We can see that present logic shows a drastic improvement in the noise metric especially for the higher fan-in cases. We get a 16.6 times improvement over conditional keeper logic and a 17.7 times improvement over standard domino logic. Thus, the proposed form of domino logic has a great potential for application in the design of high fan-in gates in the modern CMOS technology and has proven to be both noise-immune and leakage-tolerant.

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