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Physical Design of Source Couple Logic Pulse Generator Circuit for Ultra Wideband Applications

M. Azaga and M. Othman
VLSI Design Center, Faculty of Engineering, UKM, Bangi, 43600, Selangor, Malaysia

Abstract: A proposed design of Ultra Wideband (UWB) pulse generator circuit is presented. The design is based on Source Couple Logic (SCL) for its low power and high immune to noise so it can be used in mixed signal ICs environment. The pulse is digitally generated by using SCL inverters and NAND gates; the output of clock pulse input is dual pulse signals opposite to each other. The design is simulated and result of the circuit is dual pulses with width of sub-nanosecond. The results gotten have satisfied the design idea as desired. Post simulation has been carried out by using HSPICE, the layout is done using Cadence Virtuoso and verification is done by Mentor Graphic Interactive tool. All simulations are based on MIMOS 0.35 μm process PDK.

Key words: Source couple logic, ultra wide band, pulse generation circuit, analog mixed signal circuit design

INTRODUCTION

Ultra Wideband (UWB) radio is defined as a wireless technology to transmit data over very wide spectrum of frequency bands with very low power (Kim and Park, 2003). It's capable of carrying extremely high data rates over a short distance (e.g., <15 m) with very good communication features (Silverstrim, 2003; Intel, 2004; Heydari, 2007; Luo and Yang, 2003). For that UWB radio (impulse radio) becomes more interesting from industry, government and academic institutes.

The first considerations in the designing UWB circuits and system is choosing a proper impulse signal type for the UWB radio, since the impulse type determines the performance level of the UWB systems (Taylor, 1994). The selected waveform for UWB system has to provide the best transferring capacity and must have low interference characteristics to enable a high data transferring rate and wide operation range. Also, implementing the pulse circuit on a chip could be other benefits for commercial product (Jeong and Jung, 2004). Different types of pulse-generation/shaping algorithm for UWB system are proposed by Lee and Nguyen (2001), Luo and Yang (2003), Marsden and Lee (2003), Parr *et al.* (2003), Dilmaghan *et al.* (2004) and Jeong and Jung (2004), also, circuit implementation (Lee and Nguyen, 2001; Marsden and Lee, 2003; Dilmaghan *et al.*, 2004; Jeong and Jung, 2004) and coherent and noncoherent receiver architectures using these pulses have been presented by Dmitriev *et al.* (2003) and Oh *et al.* (2005). The use of digital filters in the shaping are flexible in terms of programmability, but the complexity and requirements for very high-speed clock building blocks make their implementation nontrivial. Because of the difficulties encountered in implementing digital filters, most of the pulse generation circuits are based on analog pulse generator circuit.

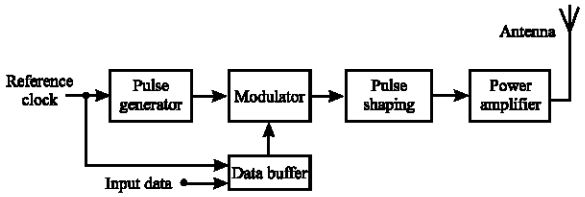

Fig. 1: Typical UWB transmitter

The typical pulsed UWB transmitter shown in Fig. 1 is composed of different basic blocks as the following: pulse generator to produce a Gaussian monocycle pulse, modulator for encoding, impulse shaping to shape the pulse to fit the FCC UWB required mask and power amplifier to amplify the modulated signal for transmitting antenna. All designed pulse generation circuit which refereed before use standard CMOS as basic building elements.

The basic concerns of this study is to design a pulse generation block with emphasis on low-power concepts and immune to digital noise in mixed signal environment. The proposed design introduces a new efficient-power, high stability pulse generator circuit using Source Couple Logic (SCL) technique by mean of delay line and, a NAND

Corresponding Author: Mohamed Azaga, VLSI Design Center, Faculty of Engineering, UKM, Bangi, 43600, Selangor, Malaysia
Tel: 0060123619460

gate. The SCL is promising high speed efficient-power consumption logic comparing to the conventional CMOS logic. It had shown to be an interesting alternative logic style than the traditional static CMOS logic in many applications (Allstot and Chee, 1993; Kundan and Hasan, 2000; Alioto and Palumbo, 2003; Khabiri and Shams, 2004; Kwan and Shams, 2004). Indeed, even if the basic drawback of SCL gates is to have static power consumption, they are faster and show a better power efficiency than standard CMOS gates in high-speed applications (Maskai and Kiaei, 1992; Allstot and Chee, 1993; Kundan and Hasan, 2000; Alioto and Palumbo, 2003). In addition, SCL gates generate a much lower switching noise, thus they dramatically reduce the digital noise induced on the analog circuits in mixed-signal applications and inherently have a better signal integrity (Khabiri and Shams, 2004; Kwan and Shams, 2004). As another potential advantage which is currently under investigation, SCL circuits have a lower sensitivity to process variations (Allstot and Chee, 1993; Srinivasan and Ha, 2004). Hence, SCL circuits are less sensitive to the limitations arising from the technology scaling; therefore, they are an interesting logic style in digital/mixed-signal ICs in sub-100 nm technologies. The output of impulse generation block is a narrow pulse that comply the UWB pulse specification (usually in rang of sub-nanoseconds (Han *et al*., 2003).

This study concern mainly the pulse generation circuit block.

PULSE GENERATION CIRCUIT

The Pulse Generation Circuit (PGC) is based on idea of comparing two pulses, one delayed to another and generating a pulse by amount of time difference in between as shown in Fig. 2. This is done digitally by means of comparing two signals, original signal and its delayed version, using NAND gate which output the difference pulse.

To implement this idea, PGC is proposed as shown in the Fig. 3, the inverter and NAND gates are designed using SCL. The PGC is composes of different blocks and parts as shown in Fig. 3. Beginning, since SCL is dual mode logic, a designed circuit is needed to change from single-mode to dual-mode logic which done by single-to-dual converter block which outputs dual opposite pulses which required by SCL. The output of pulse generator circuit is ready dual-pulse (+ve and -ve) which can be utilized for encode the transmitted data using pulse polarity coding scheme (+1 and -1) and this is considered one of the advantages of using SCL.

The input to the PGC is single clock pulse, (A in the Fig. 2) repetition frequency is converted to dual pulses as needed by SCL (B and C), the single-to-dual converter is designed by mean of CMOS inverter and Transmission Gate (TG). Figure 4 connected in parallel to get same delay on the dual opposite output signals, then, its connected to the SCL Inverter in order to get desired ΔV to other SCL gates in the PGC. To have balance switching

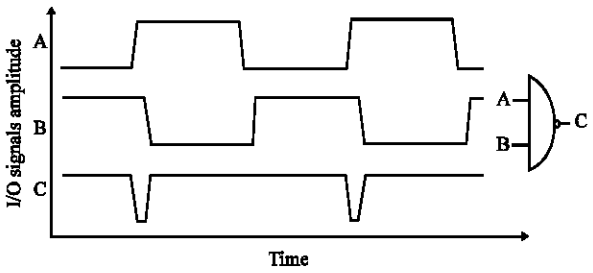

Fig. 2: Pulse generation data

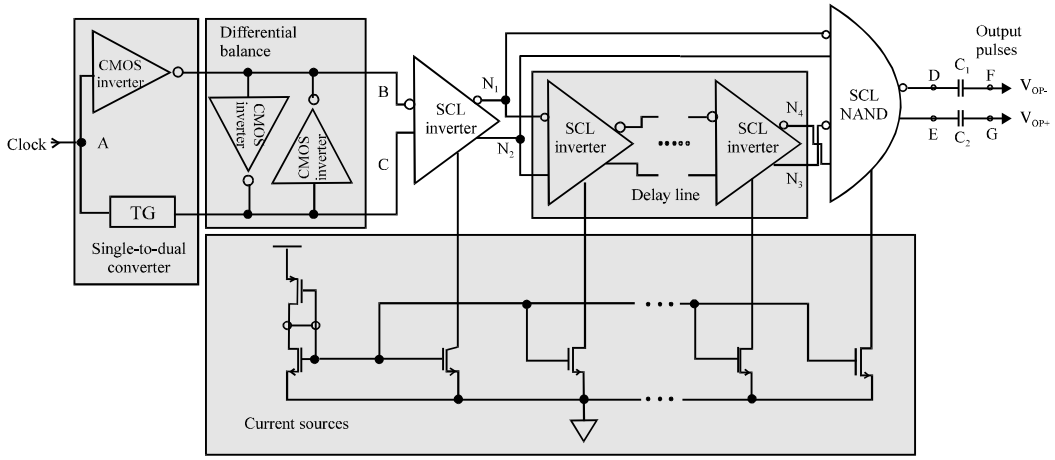

Fig. 3: Pulse generation circuit topology

and same slew rate, the outputs of single-to-dual converter block are connected differentially by means of two CMOS inverter, one opposed the other, as shown in the differential balance block in Fig. 3. The output dual-signals of SCL inverter are inputted to the delay line and SCL NAND gate at the same time. The delay line is consisting of odd/even number of SCL inverters; therefore, the output of the delay line (N_3 and N_4) is delayed inverted original input signals N_1 and N_2. The amount of delay is multiple delay of the used SCL inverter, the delay of delayed signal will give the width of output pulses from pulse generation block (D and E), since it's input to 2-inputs SCL-NAND with original dual signals (N_1 and N_2), the output of SCL-NAND will goes high as one of the input signals is low. To get inverted signal at second dual inputs of SCL-NAND for comparison, attention must be taken for connecting of N_3 and N_4 to the SCL-NAND, that is depending on the number of SCL inverter in the delay line, odd/even, if it's odd, the connection will be directly-true to true and false to false, where, if it's even, the connection will be inversed - true to false and false to true-as in Fig. 3.

The TG and CMOS inverter are shown in Fig. 4a, b sized in such a way that the output signal has same rising and falling time during switching. The schematic diagram of SCL-NAND gate used in the PG circuit is shown in Fig. 4c. The coupling capacitor C_1 and C_2 are used to remove the DC component of the output signals (F and G).

The PMOS in the inverters and NAND should be sized to get the desired output voltage swing (ΔV), where as NMOS sized to have good noise margin (Azaga and Othman, 2006). As SCL gate needs a current to be steered to one of output branches, a current mirror is used as current source connected to the SCL gates to draw the gate current. Normal current mirror is used with diode connected NMOS as current source reference for the current mirror (Allen and Holberg, 2002). The value of current is affecting the ΔV and delay of SCL gate, so, it's sited to get low gate delay and desired ΔV (Azaga and Othman, 2006).

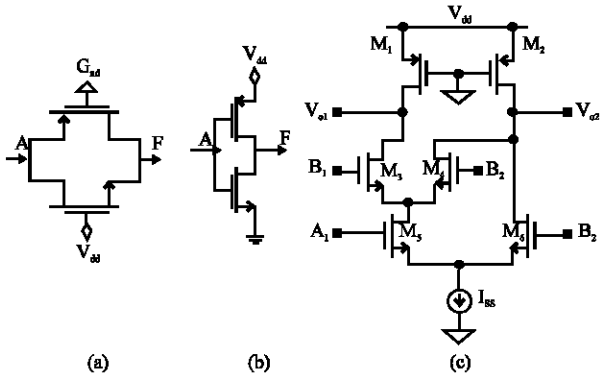

Fig. 4: (a) TG, (b) CMOS inverter and (c) SCL-NAND

PHYSICAL DESIGN OF PGC

The way of layout the SCL gates have effective affect on its performance from point of voltage swing and switching noise, signal delay, as well as utilized area, that is due of introduced RC parasitic (Azaga and Othman, 2008). Four ways of layout are suggested by Azaga and Othman (2008) for SCL gates, among them, fingering and comb layout techniques have been chosen for PGC layout as they have different parasitic effect and to investigate the influence of layout technique over the PGC output signals characteristics. The layout of PGC was done by two versions, using fingering technique (layout I) as in Fig. 5 and using comb technique (layout II) as shown in Fig. 6, which clearly illustrate the reduction of PGC size by the second layout to approximately half of the first layout. The layout is done based on 0.35 μm MIMOS PDK and using Virtuoso-Cadence, where, the extraction is done by Mentor Graphic-Caliber interactive tool.

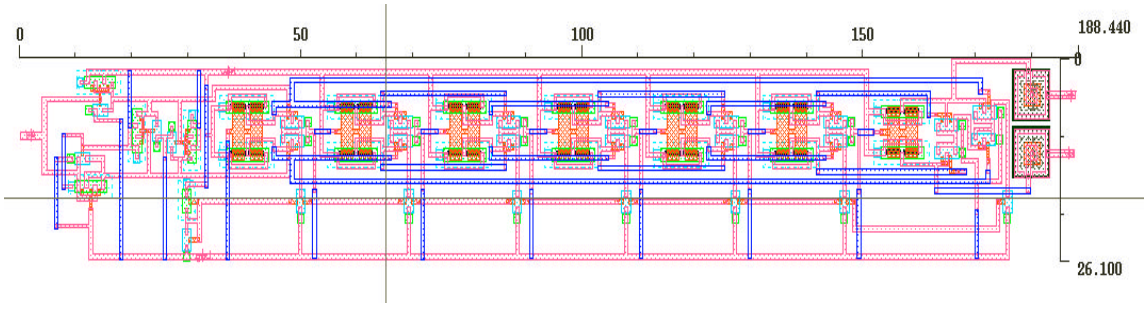

Fig. 5: Layout I: Fingering technique

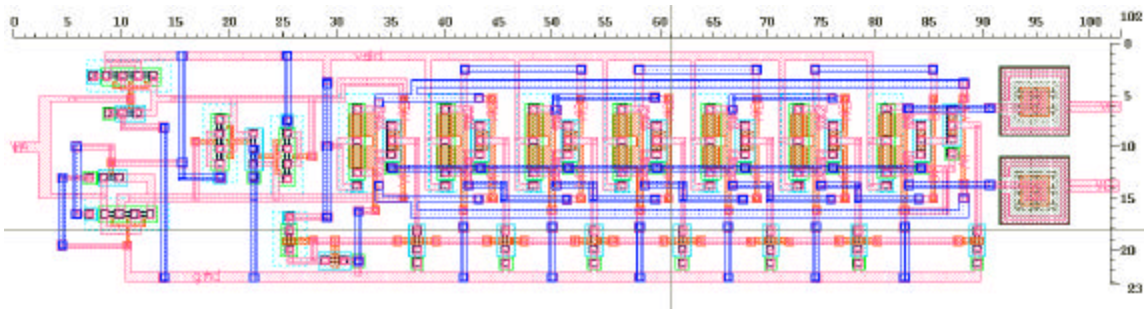

Fig. 6: Layout II: Comb technique

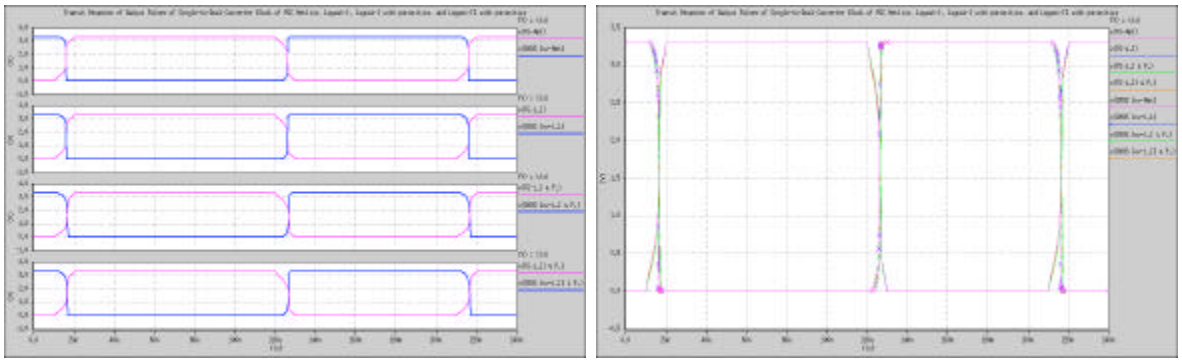

Fig. 7: (a and b) Output pulses from single-to-dual converter block for all PGC models

SIMULATION RESULTS

The PGC was designed digitally using SCL gates which considered high noise immune in the mixed signal ICs environment. Physical (Post) simulation is carried out using HSPICE on PGC netlist as well as extracted layouts. Four models of PGC has been considered in post simulation phase, PGC netlist, PGC layout-I pure, PGC layout I with added extracted parasitic and PGC layout II with added extracted parasitic, arranged, respectively where mentioned. The input reference clock pulse to the PGC (V_A) is fixed in all post simulation with frequency of 5 MHZ, 10 nsec rise/fall time, 10 nsec delay and 0 to 3.3 V voltage range. V_A is then converted to dual signals (V_B and V_C) by CMOS inverter and TG of the single-to-dual converter block, Fig. 7a and b shows the outputs of single-to-dual converter block of all PGC models.

The dual pulse signals V_B and V_C are input to a SCL inverter in order to achieve desired ΔV for subsequent PGC stages. The SCL inverter's output is applied parallel to SCL-NAND and delay line, the delay line composes of odd number of SCL inverters. At the input ports of SCL-NAND (N_1, N_2, N_3 and N_4) are the original signals and its delayed inverted copy (Dual) as shown in Fig. 8a and b.

The outputs of SCL NAND are dual inverted short impulse signals with added some DC voltage because of SCL ΔV is part of full headroom voltage. The width of output impulses is based on the amount of delay causes by the delay line to the original dual signals. The DC voltage is removed by using capacitors at the output of SCL-NAND. Figure 9a-d, shows the input/output impulse signals of capacitors for four simulations models of PGC.

The four models of PGC output four different dual short impulses, as shown in Fig. 10. The shown characteristics of PGC output signals are fitting UWB pulse duration constrain as required, but the difference in pulse characteristics are due to parasitic effect on circuit behavior. The amount of RC parasitics added to the circuit layout has major impact on signal strength and delay.

The output pulses of PGC Netlist and layout I pure are showing less delay to middle falling edge of V_A than layout I and II with parasitic, a mostly it's close to middle falling edge of V_A. The PGC Netlist is considering only the devices models as in the PDK. The peak voltage of PGC layout I pure output signals is more than PGC layout I and II with added parasitic because no parasitic capacitance/resistance is added, only the physical layout of the devices is considered with its resistance/ capacitance, which less than the total layout capacitance/

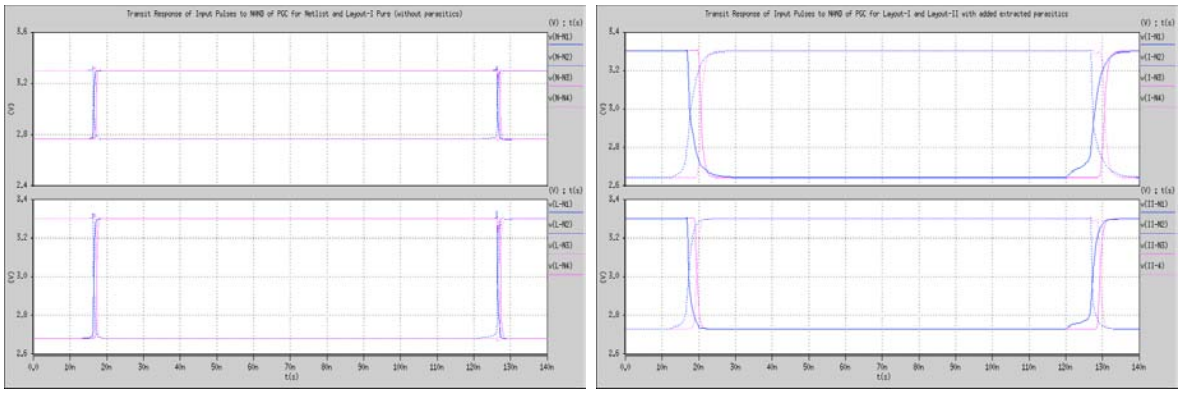

Fig. 8: (a and b) Inputs pulses to SCL NAND (N_1, N_2, N_3 and N_4) for all PGC models, Netlist, Layout-I pure, Layout-I, and Layout II, respectively

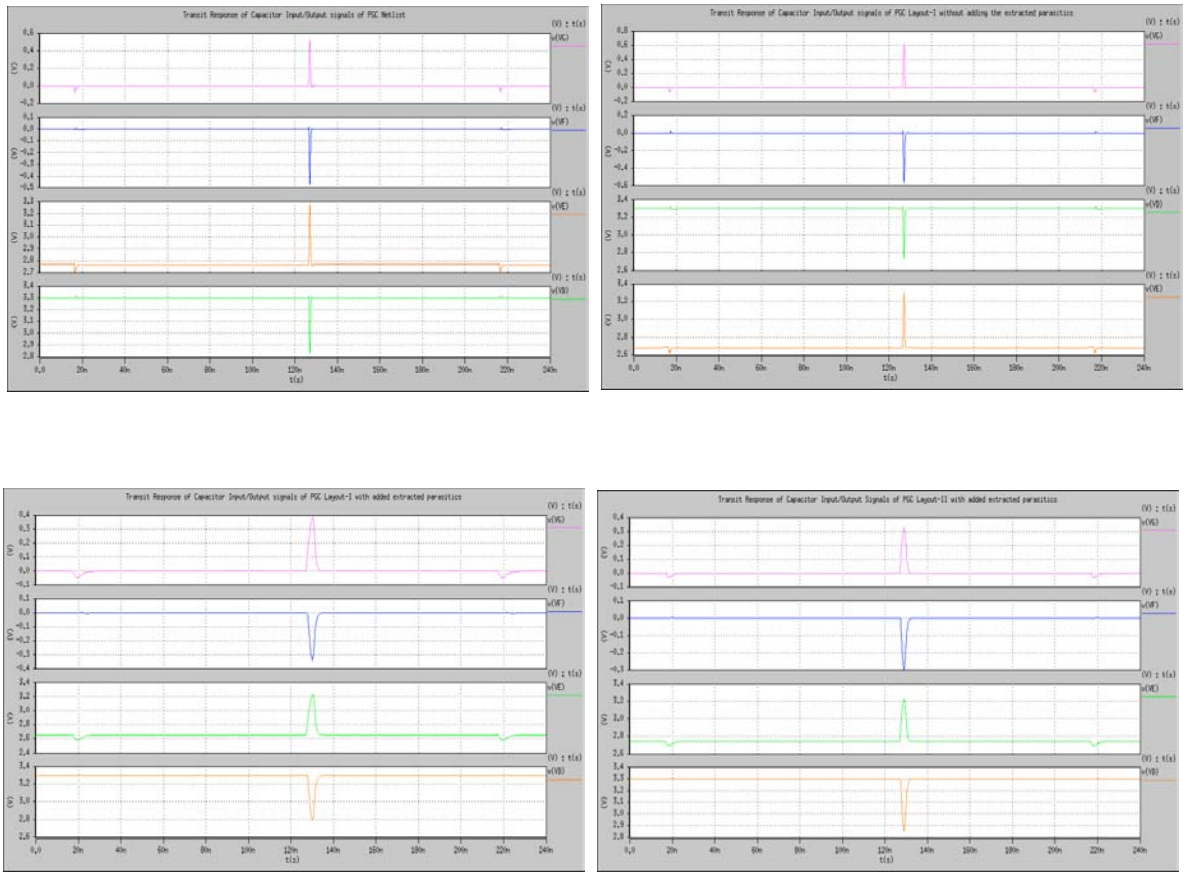

Fig. 9: (a-d) Output pulses from SCL NAND (V_G, V_F, V_E and V_D) for all PGC models, respectively

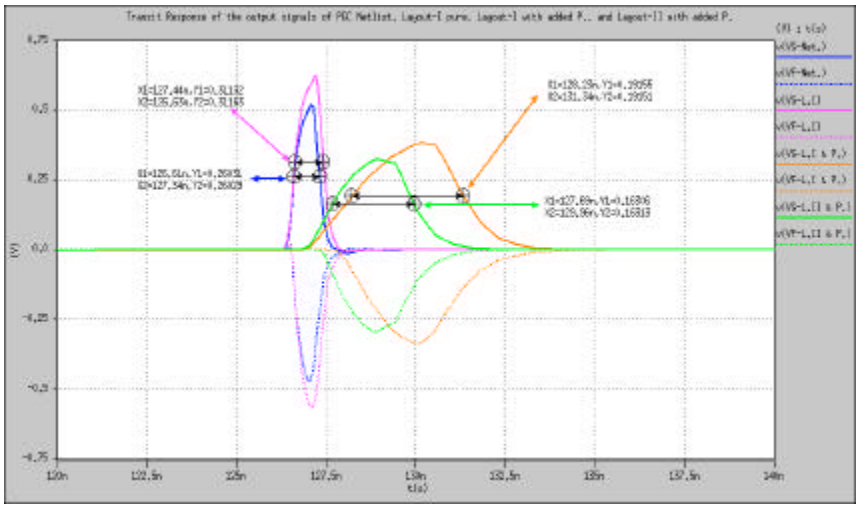

Fig. 10: The output pulses of PGC (all models)

Table 1: The main output pulses parameters of different PGC models

PGC model	Pulse peak voltage (v)	Pulse width (ns)
Netlist	0.52076	0.73
Layout I pure	0.62323	0.81
Layout I and P	0.38300	3.11
Layout II and P	0.32636	2.27

resistance parasitic, that is raise slightly the ΔV than PGC Netlist and others. PGC Layout-I with added parasitic shows more width and peak voltage of output pulses than PGC layout II with added parasitic due to increasing of it is nodes and paths capacitance as well as decreasing resistance values. Both, PGC Layout-I and Layout-II with added parasitic output signals have same delay to the V_A due of signals paths capacitance. Table 1 shows the main parameters of the four PGC models output pulse signals.

CONCLUSION

The PGC was digitally designed by using SCL gates, that suitable to use in mixed signal ICs environment. SCL inverters are used in delay line to delay the input signal, where, 2-inputs SCL-NAND were used to get difference between the original and delayed signals. In the design, 5 stages of SCL-Inverters used as delay line, the amount of delay is controlled by the total delay of the delay line and by increases the delay elements the total delay can be increased, so the output pulse width from SCL-NAND. Extensive simulation is done to adjust W/L for all CMOS in PGC blocks to get best output pulse and apply the SCL design constrains at same time. Four models of PGC are considered for investigation, two different layout techniques were considered in post simulation. The simulation results show important effect of layout on output pulses characteristics and all PGC performance. All output pulse signals of all PGC models are short impulse width in sub-nanosecond which fit the UWB pulse width constrain (Han *et al*., 2003). All post simulation is carried out by HSPICE and using MIMOS 0.35 μm process PDK. The fabrication of layout-I and layout-II PGCs is under processing and the measurements shall be discussed and explored in the further study,

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