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Applications of Evolutionary Algorithms in the Design Automation of Analog Integrated Circuits

¹E. Tlelo-Cuautle, ¹I. Guerra-Gómez, ¹M.A. Duarte-Villaseñor, ²Luis G. de la Fraga, ³G. Flores-Becerra, ⁴G. Reyes-Salgado, ¹C.A. Reyes-García and ¹G. Rodríguez-Gómez
¹INAOE. Luis Enrique Erro No. 1, Tonantzintla, 72840 Mexico
²CINVESTAV. Computer Science Department, Av. IPN 2508. 07360, Mexico
³Instituto Tecnológico de Puebla. Av. Tecnológico 420, 72220, Mexico
⁴Department of Computer Sciences, Cuernavaca, 62490, Mexico

Abstract: During the last decade, evolutionary algorithms (EAs) have shown its usefulness for solving multi-objective optimization problems. In the field of analog Integrated Circuits (ICs), they provide a set of feasible solutions for the optimal synthesis and sizing of different kinds of linear and nonlinear circuits, namely: amplifiers, filters and oscillators. The optimization of these circuits can enhance the performance for signal processing applications in electronics. In this study we present the state of the art in applying EAs for the synthesis and sizing of analog ICs. A survey of the main people working in this field and recent major advances and discoveries are summarized. Some insights on the behavior of EAs in the optimal design automation of analog ICs are given. Finally, several open research problems are listed mainly devoted to improve the electronic design automation tools for analog ICs by applying EAs.

Key words: Electronic design automation, evolutionary electronics, evolutionary algorithms, circuit synthesis, circuit sizing, genetic algorithm, non-sorting genetic algorithm, multi-objective evolutionary algorithm, unity-gain cell, current conveyor, CMOS integrated circuits

INTRODUCTION

The Electronic Design Automation (EDA) industry is focusing on providing optimal software solutions for the modeling, design and simulation of analog, digital and mixed-signal Integrated Circuits (ICs). At high-speeds and high-frequencies of operation, the digital circuits present analog behaviors, so that the EDA efforts become oriented to develop analog ICs design methodologies to compute the optimal circuit topology and sizes of a circuit to accomplish the desired target specifications.

The EDA industry has roots from nearly six decades ago. For instance, the development of computer-aided tools gained real momentum in the 1950's when electric computers were introduced and used in circuit analysis (Chua and Lin, 1975). Furthermore, circuit simulators have been used within design automation methodologies for general or specific purposes, with the same goal of generating optimal solutions. Besides, to avoid trial and error techniques and CPU-time waste during the modeling, design and simulation of ICs, different kinds of optimization procedures have been explored. In this manner, this review article summarizes the major developments in the design automation of analog ICs by

paying attention on the application of multi-objective Evolutionary Algorithms (EAs). The rest of this Review Article is devoted to present the state of the art in the Analog Design Automation (ADA) of ICs. We discuss some techniques for circuit synthesis of mixed-mode ICs and circuit sizing in general. Afterwards, we introduce the recent developments in applying EAs for the optimization of analog ICs. In the last part, we discuss some insights on the behavior of EAs in the optimal sizing of analog ICs, as well as several open research problems to improve the ADA of ICs by applying multi-objective EAs.

ANALOG DESIGN AUTOMATION

The first general-purpose circuit analysis programs emerged early 1960's (Jensen and McNamee, 1976). Among all the currently available circuit simulators, the one developed by Nagel and Pederson (1973), SPICE, has been adopted by academic researchers and many EDA industries for the modeling, design and simulation of analog, digital and mixed-signal ICs. Besides, for nanometer technologies and when the desired operations of the ICs require high-speed and high frequency, all electrical behaviors become analog (Tan and He, 2007;

Lewyn *et al.*, 2009). Therefore, in general we focus on the optimization of analog ICs by applying multi-objective EAs.

During the last decade (2000's), a lot of Analog Design Automation (ADA) tools have been developed, all of them with the main goal to find the optimal topology and transistor sizes to accomplish target requirements. For instance, Martens and Gielen (2008), presented an overview on the classification and a brief description of the majority of the design strategies supported by analog EDA tools, developed by researchers and companies in recent history over more than 20 years. The classification divided the IC design automation flow into five levels of abstraction: layout, circuit, macro-model, behavioral and functional level. In this manner, from the EDA point of view, the creation of IC architectures happens either via a top-down or a bottom-up design flow. Besides, several optimization algorithms are reviewed to determine the values of the parameters once the architecture has been chosen. Although the overview helps the analog designer to select the right approach for the right task, the analog IC design is quite complex for every specific application, so that other novel modeling, design and simulation tools are necessary to find the optimal performances of an IC.

Among the most recognized works on the ADA of ICs during 2000's, we can cite the following authors: (Aminzadeh and Lotfi, 2007; Baskaya *et al.*, 2009; Burmen *et al.*, 2002, 2004, 2008; Chang and Kundert, 2007; Chan and Zilic, 2009; Daems *et al.*, 2003; DeSmedt and Gielen, 2003; Eeckelaert *et al.*, 2004; Fakhfakh *et al.*, 2009, 2010; Garcia-Ortega *et al.*, 2007; Gielen and Rutenbar, 2000; Guo *et al.*, 2006; Hassan *et al.*, 2005; Hershenson *et al.*, 2001; Hjalmarson *et al.*, 2003; Koza *et al.*, 2004; Kranti and Armstrong, 2009; Lee and Kim, 2006; Li *et al.*, 2008; Liu *et al.*, 2008, 2009a; Lui *et al.*, 2010; Mande *et al.*, 2009; Massier *et al.*, 2008; McConaghy and Gielen, 2009a-c; Muller-L, 2009; Nguyen-Huu *et al.*, 2009; Nussdorfer *et al.*, 2007; Puhan *et al.*, 2003, 2007; Rutenbar *et al.*, 2002; Sobe *et al.*, 2009; Stehr *et al.*, 2007; Tajalli *et al.*, 2010; Tlelo-Cuautle *et al.*, 2007; Unno and Fujii, 2006, 2007; Xu *et al.*, 2009; Yilmaz and Dundar, 2009; Zhang *et al.*, 2006, 2008). The majority of these ADA approaches are based on numerical simulations. Besides, some symbolic behavioral modeling approaches have been introduced by Gielen and Rutenbar (2000), McConaghy and Gielen (2009b), Rutenbar *et al.* (2002, 2007), Tan and He (2007) and Tlelo-Cuautle *et al.* (2010c, d). These modeling techniques help the designer to get insights on the behavior of the ICs and they may enhance the optimization procedures.

Although, the ADA approaches listed above introduced solutions for many modeling, design and simulation problems in the IC industry, the optimization of nonlinear circuits and systems, e.g., (Sanchez-Lopez *et al.*, 2010; Trejo-Guerra *et al.*, 2009), yet has two main bottlenecks: the selection of the right circuit topology and the sizing of the circuit elements. For the sizing case, multi-objective evolutionary algorithms (MOEAs) are well suited to generate feasible solutions. For the topology selection, several synthesis approaches have been introduced by the following authors: (Aggarwal, 2003, 2004; Castro-Lopez *et al.*, 2008; Dastidar *et al.*, 2005; Doboli and Vemuri, 2003; Grimbleby, 2000; Ilsen *et al.*, 2008; Koza *et al.*, 2000; Massier *et al.*, 2008; Mattiussi, 2005; Mattiussi and Floreano, 2007; Mukherjee *et al.*, 2000; Munoz-Pacheco and Tlelo-Cuautle, 2009; Natsui *et al.*, 2007; Phelps *et al.*, 2000; Rutenbar *et al.*, 2007; Saad and Soliman, 2008, 2010; Salem-Zebulum *et al.*, 2002; Shibata and Fujii, 2001; Tlelo-Cuautle and Duarte-Villasenor, 2008; Tlelo-Cuautle *et al.*, 2008a, b, 2010b; Van der Plas *et al.*, 2001; Vodopivec, 2003).

Koza *et al.* (2000) presented a synthesis technique for the generation of circuit topologies and sizing by applying genetic programming. In the same year, Mukherjee *et al.* (2000) presented an approach for the efficient handling of operating range and manufacturing line variations in analog cell synthesis. These works introduced good approaches for the hard open problem related to variations in manufacturing and simulation of analog ICs. A very useful ADA tool was also presented in the same year by Phelps *et al.* (2000), Anaconda: Simulation-based synthesis of analog circuits via stochastic pattern search. At the same time, a proposal for the problem on the encoding of analog ICs was presented by Grimbleby (2000). He introduced the application of genetic algorithms for the encoding of passive filters. Further, Aggarwal (2003) applied genetic algorithms to synthesize nonlinear circuits, such as sinusoidal oscillators. In a more general sense, Mattiussi (2005), Mattiussi and Floreano (2007) and Salem-Zebulum *et al.* (2002) introduced encoding approaches for linear and nonlinear analog ICs. From these encoding approaches, it was possible to generate a variety of circuit topologies, so that an environment for ADA was able to synthesize ICs by selecting the better or best topology to accomplish, in an optimal way, target specifications. These encoding approaches opened a new research area called *evolutionary electronics* (Salem-Zebulum *et al.*, 2002; Tlelo-Cuautle and Duarte-Villasenor, 2008).

The synthesis of several active devices by applying binary genetic encoding can be found in the works of Tlelo-Cuautle and Duarte-Villasenor (2008),

Tlelo-Cuautle *et al.* (2008a, b, 2010b). In that approaches the generic analog cells are evolved to design more complex devices by superimposing of sub-circuits.

DESIGN AUTOMATION OF MIXED-MODE CIRCUITS BY EVOLUTIONARY ALGORITHMS

One of the main paradigms in biology, is the principle of evolution and how does the individuals perform changes through the time. As a result of these changes new species arise from which other ones are derived and so on. The principle of evolution has been successful applied to solve very complex optimization problems, where the traditional numerical methods does not obtain solutions, i.e., with non-continuous differentiable problems. In a wide sense, an Evolutionary Algorithm (EA) is a searching algorithm that uses combination, mutation and survival of the fitness individuals in order to solve an optimization problem.

The EAs applied to the ADA of ICs (Salem-Zebulum *et al.*, 2002) have the following characteristics: They work with a set of solutions and not with the self-solutions; they search solutions within a population of possible solutions and not with single solutions; they use an evaluation function and not using functions derived from this one or another method or similar knowledge; they use probabilistic transition rules and not deterministic ones; and they combine stochastic and direct search for elements making a notorious balance between exploitation of solutions and exploration of the search space.

If a synthesis problem is represented by a set of parameters called *genes*, when they are joined to form a string, they are called chromosomes and this process is known as encoding. For instance, it is very common that the representation of individuals is done by using binary strings, such representation is called genotype. Then, it is necessary to convert or to decode the values associated to an individual and it is called *phenotype*. A population can be formed by a set of genotypes and some genetic operations can be performed, such as: selection, crossover or recombination, mutation and elitism, re-emplacem or reinsertion. During the selection, a ranking is performed by associating the aptitude of the individuals. In evolutionary electronics, the encoding approach introduced by Tlelo-Cuautle and Duarte-Villasenor (2008), synthesizes analog ICs from the generation of Unity-Gain Cells (UGCs), namely: voltage (VF) and Current Followers (CF) and voltage (VM) and Current Mirrors (CM). Their evolution can generate mixed-mode circuits, namely: Current Conveyors (CCs) and Current-Feedback Operational Amplifiers (CFOAs). These devices are well suited for the applications presented

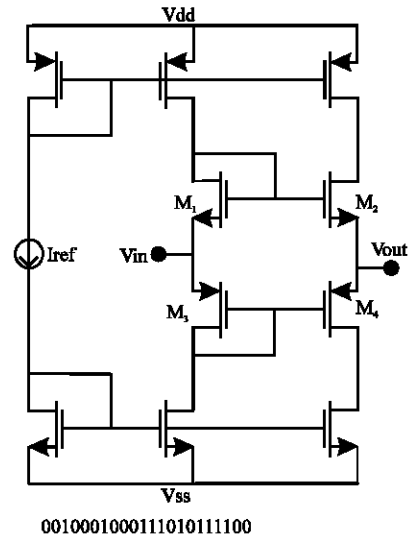


Fig. 1: Encoding a Voltage Follower (VF) and its phenotype

(Aggarwal, 2003, 2004; Garcia-Ortega *et al.*, 2007; Munoz-Pacheco and Tlelo-Cuautle, 2009; Saad and Soliman, 2008; Sanchez-Lopez *et al.*, 2008, 2010; Trejo-Guerra *et al.*, 2009).

For instance, in Fig. 1 is shown the genotype and phenotype of a Voltage Follower (VF). The application of genetic operators like crossover and mutation, leads us to the VFs shown in Fig. 2. In Fig. 2a it is highlighted that by changing one bit to the chromosome in Fig. 1, the transistor M2 changes from N-type to P-type. In Fig. 2b M2 from Fig. 1 is short-circuited between its drain and gate terminals. In Fig. 2c the transistors biasing M1-M4 change from simple Current Mirrors (CMs) to cascode CMs. Finally, in Fig. 2d, the transistor M3 from Fig. 1 is short-circuited.

The synthesis of the VFs is performed from nullator-based descriptions, as shown in Fig. 3. From these representations one can add norators (Tlelo-Cuautle and Duarte-Villasea, 2008) to form nullator-norator pairs which can be synthesized by transistors (e.g., Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)), as shown in Fig. 4, until obtaining circuits like the ones shown in Fig. 1 and 2a-d. All these process is encoded by binary strings until forming the chromosomal representation of the analog circuit.

The synthesis of the Current Follower (CF) is performed from norator-based descriptions, as shown in Fig. 5. As the dual case for the VF, from these representations one can add nullators (Tlelo-Cuautle and Duarte-Villasenor, 2008) to form nullator-norator pairs which can be synthesized by a MOSFET. The genetic algorithm for the synthesis of VFs and Voltage Mirrors (VMs) can be found in Tlelo-Cuautle *et al.* (2008b), while

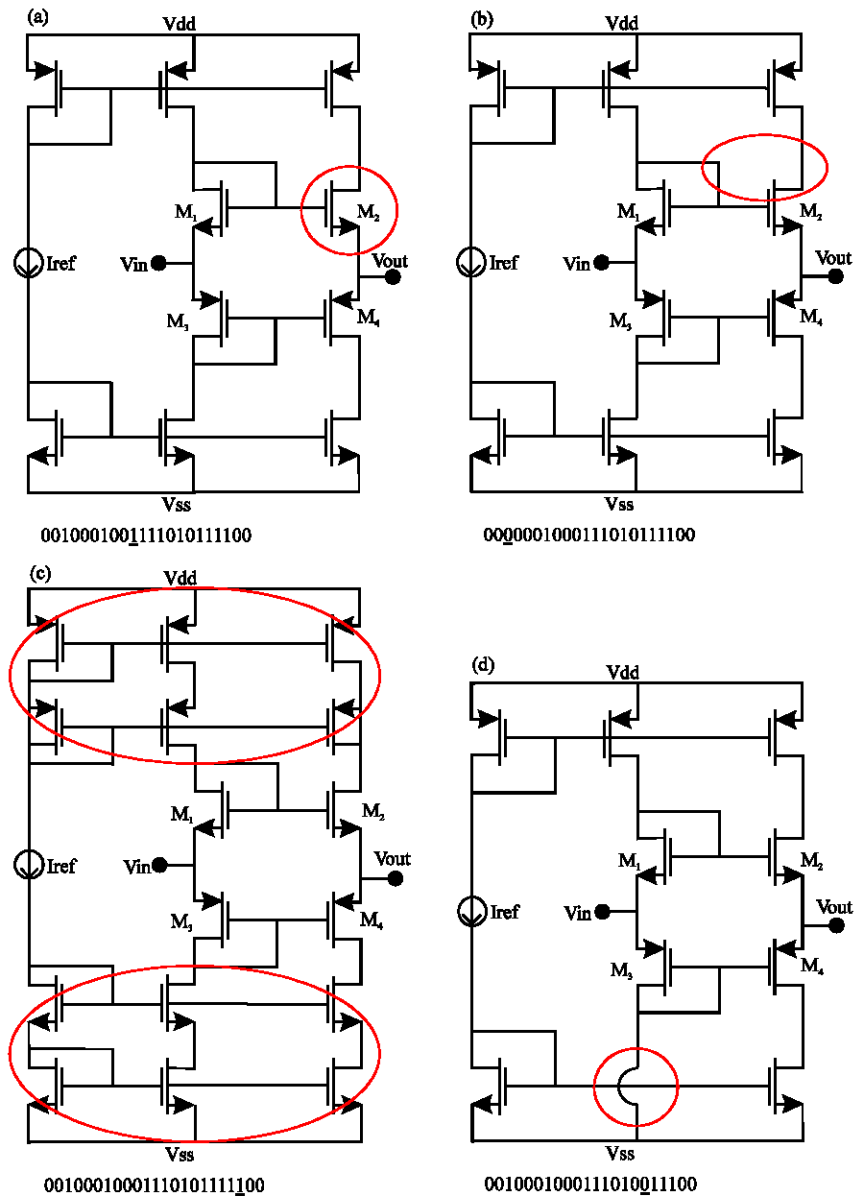


Fig. 2: VFs evolved from Fig. 1 by applying mutation operations

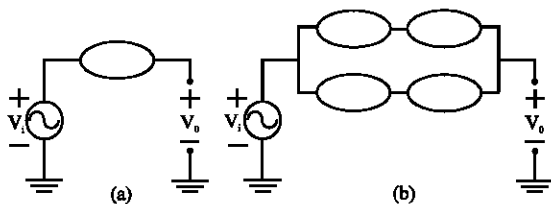


Fig. 3: Ideal representation of the VF by using (a) one and (b) four nullators (Tlelo-Cuautle *et al.*, 2008b)

the genetic algorithm for the synthesis of CFs and CMs can be found in Tlelo-Cuautle and Duarte-Villasenor (2008).

The synthesis of mixed-mode circuits can be performed by interconnecting VFs and VMs with CFs and CMs. For instance, in Fig. 6 is shown the representation of the positive-type second generation current conveyor (CCII+). As one sees, it can be synthesized from the interconnection of a VF with CMs. Lets us consider the VF shown in Fig. 1. If it is biased with ideal current sources, we get the VF shown in Fig. 7a. The evolution of the VF to generate the topology of the CCII+ is performed by the synthesis of the ideal current sources biasing M2 and M3 by using simple CMs, as shown in Fig. 7b (Tlelo-Cuautle and Duarte-Villasenoe, 2008). In a similar

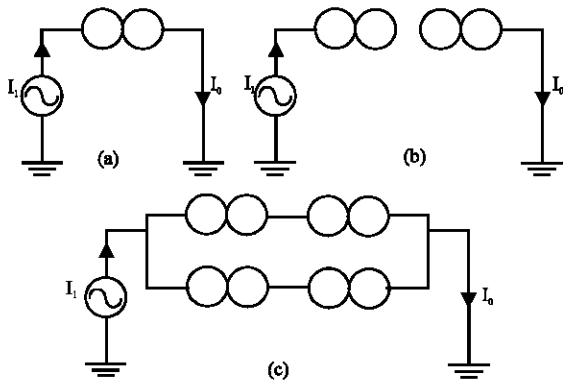


Fig. 4: Ideal representation of the CF by using (a) one, (b) two and (c) four norators

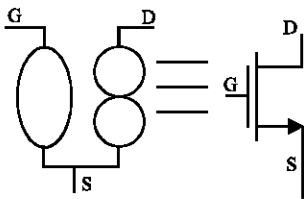


Fig. 5: Synthesis of the nullator-norator pair by a MOSFET

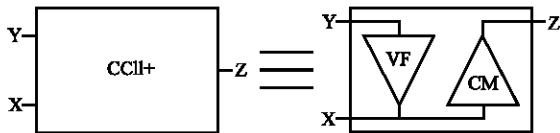


Fig. 6: Representation of the CCII+ by interconnection of a VF with CMs

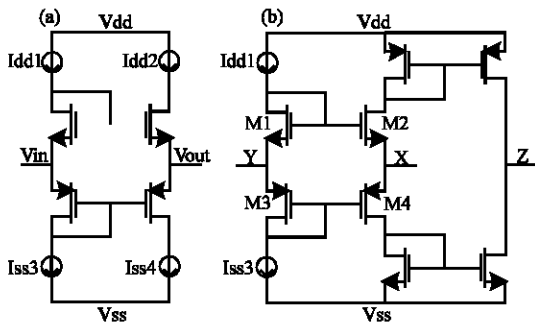


Fig. 7: (a) Description of the VF with ideal current sources and (b) description of the CCII+ from the evolution of the VF

way, the synthesis of the negative-type second generation Current Conveyor (CCII-) can be performed by super-imposing a VF with a CF, as shown in

Tlelo-Cuautle *et al.* (2008a, b). The synthesis of all kinds of current conveyors (Tlelo-Cuautle *et al.*, 2010), can be performed by interconnecting or by super-imposing the four unity-gain cells, VF, CF, VM and CM. Other mixed-mode circuits can be synthesized in a similar way. For example, the current-feedback operational amplifier (CFOA) can be synthesized by the cascade connection of a CCII+ with a VF, as shown by Tlelo-Cuautle and Duarte-Villasenor (2008). In all cases, the chromosome is represented by binary strings of different length, according to the kind of mixed-mode circuit to be synthesized.

The sizing of the MOSFETs can be performed by applying conventional optimization techniques (Chua and Lin, 1975; Aminzadeh and Lotfi, 2007; Burmen *et al.*, 2002, 2004, 2008; Chan and Zilic, 2009; Daems *et al.*, 2003; Fakhfakh *et al.*, 2009; Gielen and Rutenbar, 2000; Hershenson *et al.*, 2001; Hjalmarson *et al.*, 2003; Li *et al.*, 2008; Massier *et al.*, 2008; McConaghy and Gielen, 2009a-c; Nguyen-Huu *et al.*, 2009; Nussdorfer *et al.*, 2007; Phelps *et al.*, 2000; Puhan *et al.*, 2003, 2007; Rutenbar *et al.*, 2002, 2007; Sobe *et al.*, 2009; Stehr *et al.*, 2007; Xu *et al.*, 2009; Zhang *et al.*, 2008), by applying swarm intelligence (Fakhfakh *et al.*, 2010; Tlelo-Cuautle *et al.*, 2010b), or by applying Evolutionary Algorithms (Aguirre and Tanaka, 2003; Bao and Watanabe, 2010; Barros *et al.*, 2010; De-Arruda *et al.*, 2010; Guerra-Gomez *et al.*, 2009a-c, 2010; Liu *et al.*, 2009b; Nicosia *et al.*, 2008; Mazlumder and Rudnick, 1999; Somani *et al.*, 2007; Tlelo-Cuautle *et al.*, 2010a; Vucina *et al.*, 2010; Wang and Li, 2010; Zhang, 2010). The evolutionary algorithms based approaches are described in the following section along with multi-objective evolutionary approaches (Adeyemo and Otieno, 2009; Amiri *et al.*, 2008; Badran and Rockett, 2010; Chong *et al.*, 2007; Coello-Coello *et al.*, 2001; Dehuri *et al.*, 2007; Flores-Becerra *et al.*, 2009; Lara *et al.*, 2010; López-Jaimes and Coello-Coello, 2009; Olensek *et al.*, 2009; Otieno and Adeyemo, 2010; Xu *et al.*, 2006; Zhihuan *et al.*, 2010). The objectives to be optimized are represented and selected from the Pareto front (Graeb *et al.*, 2009; Palermo *et al.*, 2009; Liu *et al.*, 2009c; Castro-Lopez *et al.*, 2009).

EVOLUTIONARY ALGORITHMS IN THE OPTIMIZATION OF ANALOG ICS

The modeling, design and simulation of electronic circuits and systems includes multiple objectives and multiple constrains which can be accomplished by applying sizing techniques (Aminzadeh and Lotfi, 2007; Bao and Watanabe, 2010; Barros *et al.*, 2010;

$$\begin{aligned} &\text{Minimize } f(x) = (f_1(x), f_2(x), \dots, f_{10}(x))^T \\ &\text{Subject to } h_k(x) \geq 0, k = 1 \dots p, \end{aligned}$$

where, $x \in X$.

where, $X: \mathbb{R}^n | 0.36 \mu\text{m} \leq X \leq 80 \mu\text{m}$, is the decision space for the variables $x = (x_1, \dots, x_9)$ and $f(x)$ is the vector formed by ten objectives, which are evaluated as minimization functions, so that they are manipulated as follows (Tlelo-Cuautle *et al.*, 2010a):

- $f_1(x) = 1$ - Voltage gain (From port Y to port X).
The gain must be close to unity
- $f_2(x)$ = Voltage offset (Between port Y and port X).
The offset must be close to zero
- $f_3(x) = 1 / \text{Voltage band width}$ (From port Y to port X).
The bandwidth must be large
- $f_4(x) = 1 / \text{Input resistance}$ (Port Y).
The input resistance must be large
- $f_5(x)$ = Output resistance (Port X).
The output resistance must be close to zero
- $f_6(x) = 1$ - Current gain (From port X to port Z).
The gain must be close to unity
- $f_7(x)$ = Current offset (Between port X and port Z).
The offset must be close to zero
- $f_8(x) = 1 / \text{Current band width}$ (From port X to port Z).
The bandwidth must be large
- $f_9(x)$ = Input resistance (Port X).
The input resistance must be close to zero
- $f_{10}(x) = 1 / \text{Output resistance}$ (Port Z).
The output resistance must be large

Finally, $h_k(x)$, $k = 1 \dots p$ are the performance constraints. In our experiments we include the saturation condition in all transistors as constraints. As one sees, the evaluation of the objectives refers to fuzzy values, e.g., large and close to. In this case, we can apply fuzzy sets to select the feasible solutions (Flores-Becerra *et al.*, 2009). For instance, In Table 2 and 3 are listed the maximum, minimum, average value and the standard deviation of the feasible solutions, divided by five objectives for the ports Y-X (voltage-mode) and five objectives for the ports X-Z (current-mode), by applying NSGA-II and MOEA/D, respectively. These results were selected from the Pareto fronts shown in Fig. 9 and 10, respectively.

As one sees, both EAs perform a bit different. For instance, MOEA/D exhibits the best results for the offset (in voltage and current mode) and input resistance. Other results in optimizing current conveyors and mixed-mode Ics by EAs but by including differential evolution can be found in Guerra-Gomez *et al.* (2009b, 2010).

Table 2: NSGA-II optimization measurements for the CCII+

Measure	GainV (V/V)	OffsetV (V)	BWV (Hz)	RoutV (Ω)	RinV (Ω)
VOLTAGE(Y-X)					
MAX	0.9885	4.836E-3	9.733E+8	3.1576	8.115E+4
MIN	0.9758	1.105E-4	5.268E+8	0.6239	7.393E+3
AVG	0.9858	2.159E-3	7.913E+8	1.1510	2.783E+4
STD	1.947E-3	7.562E-4	1.308E+8	0.4134	1.788E+4
Measure	GainI (I/I)	OffsetI (A)	BWI (Hz)	RoutI (Ω)	RinI (Ω)
CURRENT(X-Z)					
MAX	0.9999	4.988E-5	9.425E+8	1.456E+5	13.8628
MIN	0.8513	1.972E-8	2.218E+8	7.758E+3	0.8994
AVG	0.9302	1.878E-5	4.917E+8	2.504E+4	2.5182
STD	4.140E-2	1.402E-5	1.130E+8	2.406E+4	2.4096

Table 3: MOEA/D optimization measurements for the CCII+

Measure	GainV (V/V)	OffsetV (V)	BWV (Hz)	RoutV (Ω)	RinV (Ω)
VOLTAGE (Y-X)					
MAX	0.9897	6.129E-3	9.734E+8	20.8758	1.011E+5
MIN	0.9592	7.773E-7	2.650E+8	0.5303	6.552E+3
AVG	0.9856	1.548E-3	7.268E+8	1.7078	5.037E+4
STD	5.076E-3	1.108E-3	1.551E+8	2.1357	2.873E+4
Measure	GainI (I/I)	OffsetI (A)	BWI (Hz)	RoutI (Ω)	RinI (Ω)
CURRENT(X-Z)					
MAX	1.0000	4.994E-5	9.832E+8	5.142E+5	65.3312
MIN	0.8514	6.135e-010	1.175E+8	6.641E+3	0.6405
AVG	0.9605	1.421E-5	5.175E+8	3.251E+4	4.2372
STD	4.911E-2	1.392E-5	1.680E+8	5.645E+4	8.3924

OPEN RESEARCH PROBLEMS IN ANALOG ICs OPTIMIZATION

This Review Article included a summary on the development, during the last decade, related to the Electronic Design Automation (EDA) of analog Integrated Circuits (ICs). We presented the state of the art in applying EAs for the synthesis and sizing of analog ICs along a survey of the main people working in this field. Furthermore, we summarized the application of EAs for solving the multi-objective optimization problem in sizing analog ICs. Finally, in this section we list several open research problems to improve the EDA tools for sizing analog ICs by applying multi-objective EAs.

Few years ago, Coello-Coello (2005) presented some trends in evolutionary multi-objective optimization (EMO), including algorithms, metrics, test functions and theoretical foundations. He listed an important contribution through the selection of Differential Evolution (DE) as genetic operator, which improves the convergence, diminishes errors and improves the runtime. This is very useful in the sizing of analog ICs, as recently shown by Guerra-Gomez *et al.* (2009, 2010). However, even using DE yet we cannot mention which EA performs better in sizing different kinds of analog ICs. This has been proved by Tlelo-Cuautle *et al.* (2010a), where the non-sorting genetic algorithm (NSGA-II) and the multi-objective evolutionary algorithm based on decomposition (MOEA/D) were applied in the sizing of mixed-mode analog ICs, which were encoded with up to 12 objectives and 15 variables. The results showed that MOEA/D found the best results in the majority of cases.

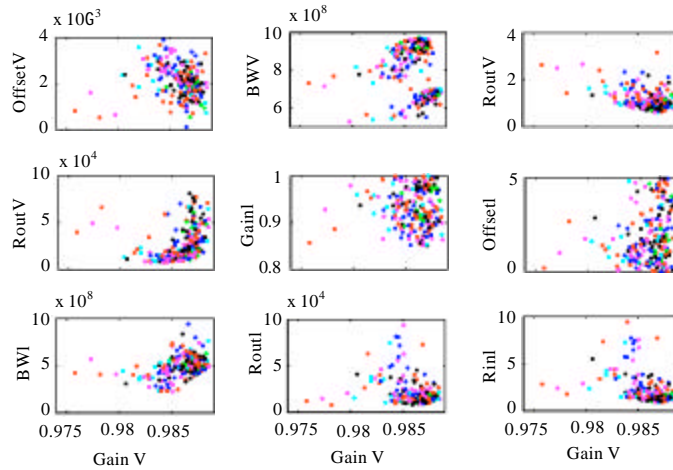


Fig. 9: NSGA-II optimization results for the CCII+, by considering the voltage gain as the main objective

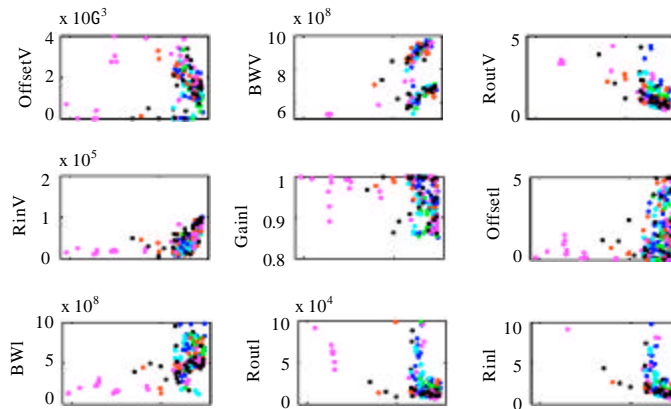


Fig. 10: MOEA/D optimization results for the CCII+, by considering the voltage gain as the main objective

Besides, in both EAs the sizing relationships W/L (width/large of the transistors) were too similar, so that both EAs found the optimal solutions in the same region of the searching space, but NSGA-II exhibited more symmetry, denoted by its statistical standard deviation. That way, an open problem is related to define the bounds of the search space to ensure that the optimal solutions are feasible. In the same direction, the design of analog ICs is not free of process variations, so that it is necessary to codify the circuit variability, because an optimal solution might be in a delicate point which does not support the natural variations of a fabrication process. This problem is related to the computation of the bounded Pareto front. Another more important open problem is the tuning of the multi-objective EAs to deal with different kinds of ICs and for different IC technologies, mainly for nanometer technologies

(Lewyn *et al.*, 2009), because the performances of the analog ICs do not scale with the scaling of the W/L dimensions of the transistors and because the high parameter dimensionality can introduce significant complexity and may even render variation-aware performance analysis and optimization completely intractable (Feng and Li, 2009).

By supposing that in sizing analog ICs we can find sets of feasible solutions (Zitzler *et al.*, 2010), the best sizing vectors can be selected by applying fuzzy-sets, as shown by Flores-Becerra *et al.* (2009). This is also an open problem during the selection, because as shown in the previous section, some objectives do not have finite bounds and they can be labeled as large (tending to infinity) or close to (tending to a finite value). In this manner, fuzzy sets can be applied to represent the large parameters (e.g., bandwidth) and some parameters such as

the gain which must be close to unity, but not zero or unity. Furthermore, the fuzzy-sets intersection is not a trivial task and it highly depends on the Pareto front. An extension of this open research problem on the selection of the best feasible solutions includes all the variants in generating the Pareto front. In this manner, to approximate a Pareto-optimal set, yet some heuristics are needed for the mating selection and variation into the populations (Guerra-Gomez *et al.*, 2010) and by taking into account multiple objectives, e.g., more than 12, as for the circuits sized in Tlelo-Cuautle *et al.* (2010a). Finally, measures to evaluate the effectiveness of generation and selecting the best Pareto-optimal performances, can be considered as general open problems in solving multi-objective optimization problems by applying EAs.

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