# Journal of Applied Sciences

ISSN 1812-5654

science alert

ANSInet
an open access publisher
http://ansinet.com

Journal of Applied Sciences 13 (9): 1602-1606, 2013
ISSN 1812-5654 / DOI: 10.3923/jas.2013.1602.1606


# Implementation of the Power Harmonic Measurement Based on FFT and DSP

[1]Tang ZhiHui and [2]Guang JianShe
[1]Department of Computer and Information Science, City College,
Dongguan University of Technology, Dongguan 523106, China
[2]College of electrical and information engineering college, Hunan University, Changsha, China

**Abstract:** Recent years with the power electronic devices was widely used harmonic became one of the main factors of affecting power quality. This paper provided a design of DSP-based harmonic detector with the characteristics of real-time and high-precision. The adding Hamming window FFT (Fast Fourier transform) algorithm was used to analyze harmonic. This paper introduced the radix-2 FFT algorithm and the performances of Hamming window function and focused on the design of the system hardware and software. The final testing results showed that the adding Hamming window FFT has good harmonic detection performance and it can depict truly the signal singularity, clear the occurring time of interference and the degree of disturbance.

**Key words:** Power quality, harmonic detection, DSP, FFT, hamming window

## INTRODUCTION

With the rapid development of economy and the wide application of the new power electronic equipment, power quality problems become the important problem of power supply system. Equipments such as Electric arc furnace, electrified railway and home switching electronics etc. will cause serious harmonic pollution in power system. Harmonic will consume reactive power and led to voltage decrease, fluctuation and distortion and increase the transmission loss (Tang *et al*., 2010; Xiao, 2004; Jiao *et al*., 2011). In industrial production, the power quality problems are often caused by harmonic. The first step for harmonic control is harmonic detection. Real-time, accurate detecting harmonic is a guarantee for harmonic control. This paper provided a design of a harmonic detector which used DSP as the central processor (Lakshmikanth and Morcos, 2001) and adopt Hamming window FFT to acquire high-precision.

## HARDWAREDESIGN

The system block diagram of the harmonic detector was designed as Fig. 1. It was consist of three parts: frequency synchronous module, signal sampling module and digital signal processing module (Wang *et al*., 2004). The three-phase voltages and currents were transformed to small voltage signals by the transformers, then the 6 channel signals were filtered to remove the aliasing components and changed by the signal pretreatment module into the voltage range which was required by the

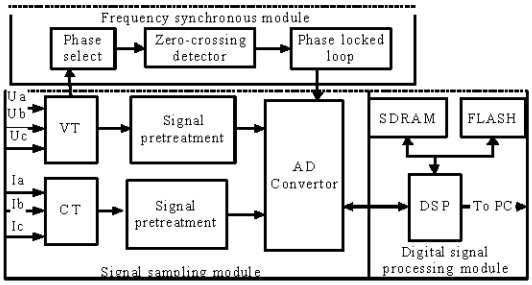


Fig. 1: System block diagram

A/D. The 6 channel bipolar signals were transformed to unipolar signals and converted to digital signal before they were processed by DSP. After processing by DSP, the results would be sent to PC through HPI bus for further processing.

The design used the ADS8365 of Taxes Instrument as A/D converter. It's a 256kSPS, 16bit, 6-channel simultaneous sampling A/D converter. The maximum sampling rate can reach 250 Ksps

When the external input clock is 5 MHz and each input channel has 300 MHz bandwidth and the transformation time is only 4 us, which can well meet the needs of the real-time sampling system.

The TMS320C5510A of TI was used as main processor. It's highly efficient, low power consumption, 16-bits fixed-point DSP chip. It has 160K×16bit high speed RAM, 6.25 ns/5 ns of instruction execution time, 160/200 MHZ clock frequency, two 20 bits counters, 6 channels DMA controller etc., so it is capable to fulfill the

**Corresponding Author:** Tang ZhiHui, Department of Computer and Information Science, City College,
Dongguan University of Technology, Dongguan 523106, China

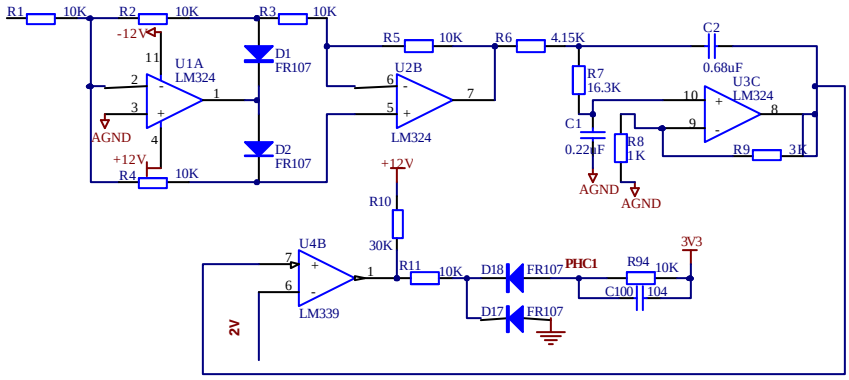


Fig. 2: Loss of phase judgment circuit

request of harmonic detector either on the time complexity or the space complexity.

**Frequency synchronous module:** The FFT algorithm is used to analyze harmonic in the design, but the key of the FFT is to reduce the spectral leakage and picket -fence effect. Frequency synchronization module was the key component to reduce picket-fence effect and guarantee the high-precision of FFT. The work role of the module was to trace the fundamental frequency of power system and use it to control the sampling frequency of A/D converter to achieve synchronous sampling. The module was consist of three parts: zero-crossing detector, phase selector and Phase Locked Loop (PLL). Zero-crossing detector transformed the voltage signal into square wave signal which has the same frequency as the voltage signal. The phase locked loop multiply the frequency of the square wave and the multiplier should be set as how many times we need sample in one signal period, thus the synchronous sampling was guaranteed. The phase selector would enhance the robust of synchronous sampling signal module. It selected one of the A, B, C phase frequency to achieve synchronous sampling signal According to the order A, B, C phase, If all the three-phase were cut off it would send an interruption to DSP to notice the user some faults has happened. Figure 2 shows the loss of phase judgment circuit.

**FFT algorithm:** The FFT algorithm is commonly used in harmonic detection. In the case of A phase voltage, The discrete FFT voltage is as follows (Oppenheim and Shafer, 1989):

$$U_k = \sum_{i=0}^{N-1} U(i) e^{-j\frac{2\pi i}{N}k}$$

If $W_N = e^{-j\frac{2\pi}{N}}$, then:

$$U_k = \sum_{i=0}^{N-1} U(i) W_N^{ik} \quad (1)$$

The radix-2 FFT algorithm is as bellow:

$$\begin{aligned} U_k &= \sum_{i=0}^{N-1} U(i) W_N^{ik} \\ &= \sum_{i=0}^{N/2-1} U(2i) W_N^{2ik} + \sum_{i=0}^{N/2-1} U(2i+1) W_N^{(2i+1)k} \\ &= \sum_{i=0}^{N/2-1} U(2i) W_{N/2}^{ik} + W_N^k \sum_{i=0}^{N/2-1} U(2i+1) W_{N/2}^{ik} \\ &= \mathbf{DFT\ (N/2_{偶数})+W_N^k\ \ DFT\ (N/2_{奇数})} \end{aligned} \quad (2)$$

Due to $W_N^{(k+N/2)} = W_N^{N/2} W_N^k = -W_N^k$, the results as bellow can be derived:

$$\begin{aligned} U_{k+N/2} &= \sum_{i=0}^{N-1} U(i) W_N^{i(k+N/2)} \\ &= \sum_{i=0}^{N/2-1} U(2i) W_N^{2i(k+N/2)} + \sum_{i=0}^{N/2-1} U(2i+1) W_N^{(2i+1)(k+N/2)} \\ &= \sum_{i=0}^{N/2-1} U(2i) W_{N/2}^{i(k+N/2)} + W_N^{k+N/2} \sum_{i=0}^{N/2-1} U(2i+1) W_{N/2}^{i(k+N/2)} \\ &= \sum_{i=0}^{N/2-1} U(2i) W_{N/2}^{ik} - W_N^k \sum_{i=0}^{N/2-1} U(2i+1) W_{N/2}^{i(k+N/2)} \\ &= \mathbf{DFT\ (N/2_{偶数})-W_N^k\ \ DFT\ (N/2_{奇数})} \end{aligned} \quad (3)$$

According to the above derivation, we can find out just the symbol of odd terms changed in the calculation of the two harmonic which have N/2 times difference. In this

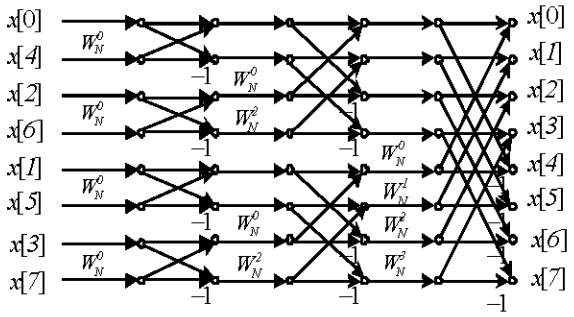


Fig. 3: The radix-2 FFT algorithm structure diagram

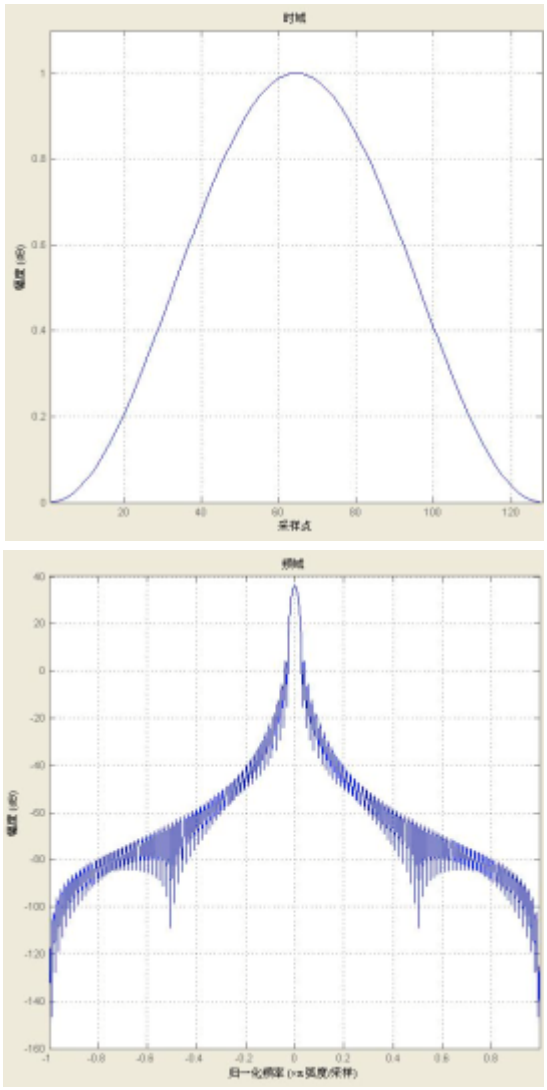

Fig. 4: Graphics of the Hamming window function

way, N/2 point subsequence can be further decomposed into two N/2 point subsequence and the FFT algorithm can be gotten just repeatedly. The radix-2 FFT algorithm decomposition diagram is shown as Fig. 3.

Add window FFT was used in the design to reduce the spectral leakage (Harris, 1978). If the rectangular window was used to truncate the signal the leakage of main lobe to side lobe would up to -13dB. Hamming window was used in the design. The maximum leakage of main lobe to side lobe is.

-31 dB and the leakage to the far side lobe would fall at the speed of -6 dB per lobe. By the way, the coherent gain of Hamming window is 0.5 and rectangle window is 1. Coherent gain indicates how much influence is made on the amplitude of the output signal by adding window FFT. The Hamming window function is as formula (4) and it's graphics of time and frequency domain is as Fig. 4:

$$\omega_H(n) = [0.5 - 0.5\cos(\frac{2\pi n}{N-1})] \quad (4)$$

The calculation formula of harmonic frequency resolution is as bellow:

$$F_0 = \frac{f_s}{N} = \frac{1}{NT} = \frac{1}{T_0} \quad (5)$$

$T_0$ indicates the time length of the data processed by a FFT computation. For example, the sampling frequency is 12.8 kHz in the design and a FFT was made every 1024 points, then the frequency resolution is as bellow:

$$F_0 = \frac{12800}{1024} = 12.5\text{Hz} \quad (6)$$

That means the frequency interval is 12.5 Hz between every two consecutive points.

## SOFTWAREDESIGN

The software design is based on the DSP/BIOS real-time kernel and includes the driver program module, interruption program module, power quality parameters calculation program module (including RMS voltage and current, three-phase imbalance, power, flicker, harmonic measurement, etc.) and the main program. Figure 5 shows the software structure and Figure 6 shows DSP main program flow chart.

**FFT program:** The key of software design in harmonic detector was the implementation of windowed FFT and the FFT algorithm including two important parts: the butterfly computation and bit-reversed addressing.

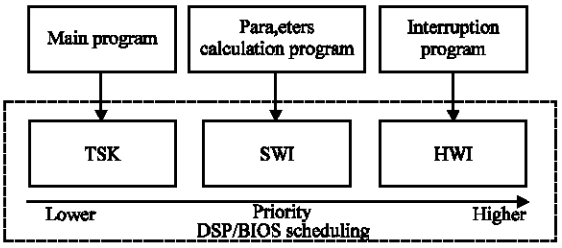


Fig. 5: Software structure

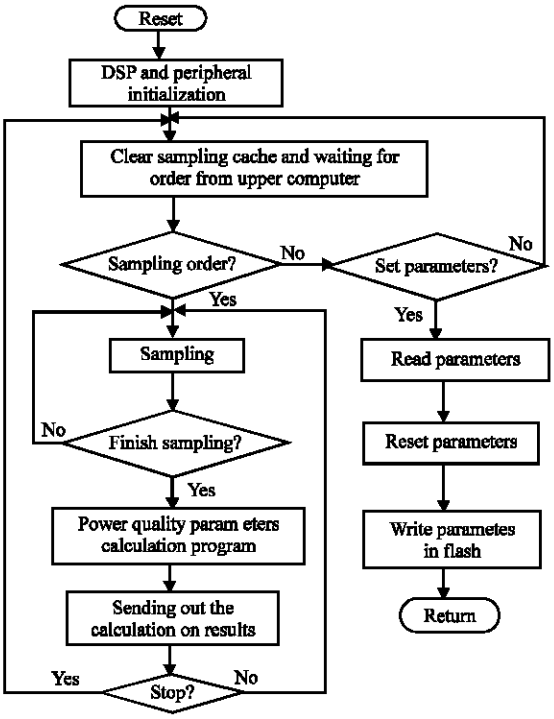


Fig. 6: DSP main program flow chart

**Butterfly computation:** The Fig. 7 shows the butterfly computation program flow chart:

For N = $2^M$ point FFT. Firstly the data was multiplied by window array w(i) stored in advance, then the butterfly calculation would be done. The program flow was consists of 3 loops. L was used in the first loop to control the order of butterfly and the distant between two node of the butterfly. There were totally M butterfly in the algorithm and M/2 nodes in each butterfly. K was used in the second loop to control twiddle factor which was changed by k and L. Both i and j were used in the third loop to control the address of the two nodes. In order to optimize the program the look-up table was used for getting twiddle factor. We should notice that all of the algorithm in the programming should be complex operation and the last results of butterfly computation should divided by 0.5 the coherent gain.

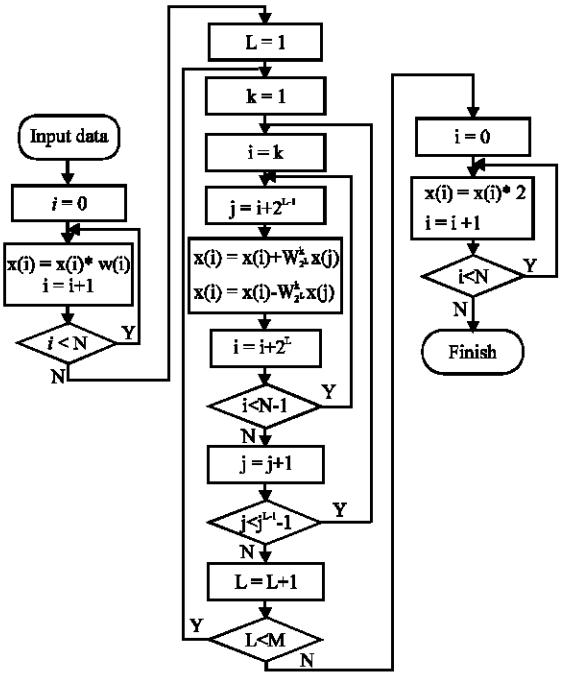


Fig. 7: Butterfly computation flow chart

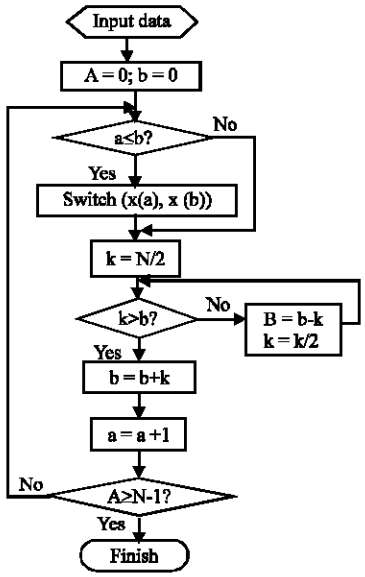


Fig. 8: Reder algorithm flow chart

**Bit-reversed addressing:** Because the butterfly computation will change the positive sequence signal into the reversed sequence spectrum, the signal data need be changed from positive sequence into reversed sequence by Bit-reversed addressing before the butterfly computation and the positive sequence spectrum could be gotten after FFT. Reder algorithm was used in the design. Figure 8 shows the program flow. N represents the

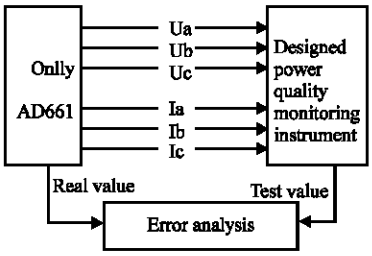


Fig. 9: Test frame

Table 1: Voltage harmonic test (unit: V)

| Input AC voltage | 3 | 5 | 10 | 20 |
|---|---|---|---|---|
| Second harmonic test value | 3.0 | 5.0 | 9.99 | 20 |
| Third harmonic test value | 2.99 | 4.99 | 9.99 | 19.99 |
| Forth harmonic test value | 2.99 | 4.98 | 9.97 | 19.96 |
| Fifth harmonic test value | 2.99 | 4.98 | 9.96 | 19.94 |
| Sixth harmonic test value | 2.99 | 4.98 | 9.95 | 19.92 |
| Seventh harmonic test value | 2.98 | 4.97 | 9.94 | 19.89 |
| Eighth harmonic test value | 2.98 | 4.95 | 9.90 | 19.85 |
| Ninth harmonic test value | 2.97 | 4.93 | 9.86 | 19.78 |
| Tenth harmonic test value | 2.96 | 4.90 | 9.79 | 19.71 |

Table 2: Current harmonic test (unit: A)

| Input AC current | 0.1 | 0.25 | 0.5 | 1 |
|---|---|---|---|---|
| Second harmonic test value | 0.10 | 0.25 | 0.5 | 1 |
| Third harmonic test value | 0.099 | 0.249 | 0.499 | 0.999 |
| Forth harmonic test value | 0.099 | 0.249 | 0.498 | 0.998 |
| Fifth harmonic test value | 0.099 | 0.249 | 0.497 | 0.997 |
| Sixth harmonic test value | 0.098 | 0.247 | 0.495 | 0.994 |
| Seventh harmonic test value | 0.098 | 0.246 | 0.493 | 0.989 |
| Eighth harmonic test value | 0.097 | 0.244 | 0.490 | 0.983 |
| Ninth harmonic test value | 0.097 | 0.243 | 0.486 | 0.976 |
| Tenth harmonic test value | 0.096 | 0.240 | 0.481 | 0.968 |

data length, a represents the addressing pointer of positive sequence and b represents the addressing pointer of reversed sequence.

## TESTS AND RESULTS

The ONLLY-AD661 Relay protection tester was used to test the designed power quality monitoring instrument, The device has four 0 ~ 125V AC voltage source and six 0 ~ 40A AC current source and their accuracy less than 0.01% measurement range plus 0.1% readings; The output frequency range is 0 ~ 1 KHZ and frequency accuracy less than 0.005 Hz. By the way, as a signal generator for test, it's voltage, current, frequency, active power, reactive power, power factor, harmonic, harmonic distortion rate, three-phase imbalance degree are adjustable. Figure 9 shows the test frame.

In voltage harmonic test, second to tenth harmonics was respectively added to a voltage signal with the amplitude 100V and the frequency 50 Hz. In current harmonic test, second to tenth harmonics was respectively added to a current signal with the amplitude 5A and the frequency 50Hz. Table 1 and 2 showed the average results of the three channels $u_a$, $u_b$, $u_c$ or $i_a$, $i_b$, $i_c$ which represents three phase voltages or currents of the real power.

The tests results showed that the measuring error increased with the harmonic order, especially above sixth harmonic. It means that the high frequency performance of the designed instrument is not very good and the frequency characteristic of the front-end analog circuit need to be further improved.

## REFERENCES

Harris, F.J., 1978. On the use of windows for harmonic analysis with the discrete fourier transform. Proc. IEEE, 66: 51-83.

Jiao, D.S., D.L. Lu and J.H. Ying, 2011. Design and implementation of a real-time monitoring system of dynamic power quality. Power Syst. Technol., 35: 110-114.

Lakshmikanth, A. and M.M. Morcos, 2001. A power quality monitoring system: A case study in DSP-based solutions for power electronics. IEEE Trans. Instrum. Meas., 50: 724-731.

Oppenheim, A.V. and R.W. Schafer, 1989. Discrete-Time Signal Processing. Prentice-Hall, Englewood Cliffs, USA., ISBN-13: 9780132162920, Pages: 879.

Tang, Z.H. and Y.F. Luo and Z. Zeng, 2010. Online electrical energy quality monitoring instrument based on dual-CPU. Low Voltage Apparatus, 15: 18-20.

Wang, B., Z.C. Pan and H.F. Zhang, 2004. Design of distributed power quality monitoring system hardware. Autom. Electr. Power Equipment, 24: 7-12.

Xiao, X.N., 2004. Analysis and Control of the Power Quality. China Electric Power Press, Beijing, China.