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FPGA Implementation of Low Power Digital QPSK Modulator Using Verilog HDL

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Abstract: Quadratute Phase Shift Keying (QPSK) is a modulation scheme commonly used in wireless communication system due to its ability to transmit twice the data rate for a given bandwidth. Even though the QPSK modulator consumes less power in a present devices but for a system such as satellite and mobile devices where their operations are power limited, this is an issue that needs attention. The objective of this study is to develop an implementable QPSK modulator that uses less power for operation. The proposed technique uses data stored inside a memory block to produce a symbol according to the input data. On the contrary, the conventional QPSK demodulation process requires a Direct Digital Synthesizer (DDS) to produce sinusoidal waveform and mixers to produce a symbol according to the input data. The proposed modulator successfully modeled with verilog Hardware Description Language (HDL), simulated with Xilinx Integrated Software Environment (ISE) version 12.4 software and implemented on Spartan 3E board. At the same time a QPSK demodulator has been developed using MATLAB tool in order to verify the functionality of the modulator. The measured performances of the modulator show the proposed architecture consumes significantly less 32 mw in total from the conventional architecture. The novelty of this work is that the researchers have focused on new methodology on reducing the modulator operational power. As a conclusion, the proposed architecture is not only able to operate as conventional QPSK modulator but at the same time significantly consumed less operation power.

Key words: Quadratute phase shift keying, Verilog hardware description language, modulator, demodulator

INTRODUCTION

Wireless communication is one of the most vibrant areas in communication field today. This is due to the increase in demand for communication connectivity driven mainly by cellular telephony and wireless data applications. Wireless communication systems require high data rate for efficient transmission of information. Several factors contribute to achieve this and one of the factors is modulation technique. Modulation techniques able to increase data transmission rate within the same bandwidth (Roddy, 2006). One of the common modulation methods used in communication system is Quadratute Phase Shift Keying (QPSK) that is part of Phase Shift Keying (PSK) modulation scheme. QPSK is widely used in wireless Local Area Network (LAN) communication, satellite communication system, Video conferencing and other forms of digital communication over a Radio Frequency (RF) carrier (Kao, 2002; Misra, 2004). Even though QPSK transmit low symbol rate when compared to other digital modulation technique such as Quadrature Amplitude Modulation (QAM) 32 and QAM 64, but it consume less power and the receiver circuit is less complex (Aspel, 2004). In QPSK modulation, the phase changes according to the input data while the frequency and amplitude remain unchanged. The quadrature in QPSK means 4 different states where every state is represented by a group of 2 bits input. The group of 2 bits can be a combinational of 00 (0), 01 (1), 11 (3) or 10 (2) and each of them will take a state as shown in Fig. 1 where the first bit represent the in-phase(I) components and the second bit represent the quadrature (Q) components.

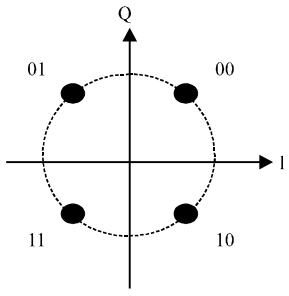

Fig. 1: Constellation diagram for QPSK

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The QPSK modulation is formed from 2 separate Binary Phase Shift Keying (BPSK) signals that combined into one. However, in QPSK the data transmission is enhanced while the Bit Error Rate (BER) over the Signal to Noise Ratio (SNR) is maintained at the same level with the original BPSK (Tahir and Zhao, 2009; Taggart and Kumar, 2011). The symbol period for QPSK signal is 2 times the bit period, $T_S = 2T_b$ while for BPSK signal the symbol period is same as bit period $T_S = T_b$. According to Kang (2009) and Elamary *et al*. (2009) implementing the QPSK signal in full digital domain not only can save cost for long term but at the same time, it increases the wireless data immunity over surrounding noise.

CONVENTIONAL QPSK MODULATOR

According to Elamary *et al*. (2009), the conventional QPSK modulator operates by dividing the info data into 2 main streams, even and odd. The divided uni-polar data then changed into bipolar by using Non Return Zero (NRZ) encoding technique. Continuously, the coded data will be mixed with carrier which is generated from Direct Digital Synthesizer (DDS) or also known as Direct Digital Frequency Synthesizer (DDFS) as shown in Fig. 2. The DDS produces the sine and cosine as separate carrier signal with same frequency. After mixing the carrier with the bipolar data, the odd data will be known as I phase and the even data as Q phase.

Table 1 shows the even and odd data represented by I and Q phase. These two phases will be added together to produce a single QPSK signal. The general mathematical form of QPSK signal, Q(t) can be expressed as shown in Eq. 1 where f_c is carrier frequency, E_S is energy per-symbols and T_S is symbol period:

$$Q(t) = \sqrt{\frac{2E_S}{T_S}} \cos\left(2\pi fct + \frac{(2i-1)\pi}{4}\right) \quad (1)$$

where, i =1, 2, 3, 4.

PROPOSED QPSK MODULATORS

The proposed QPSK modulator is a fully digital building block and will produce QPSK signal as described in Eq. 1. The overall design process is divided into 2 steps. In the first step, data for sine and cosine wave is collected from DDS by using a verilog test bench file. Next, the I and Q phase is generated from the sine and cosine data as shown in Table 2. For I phase which represent the even data, bit 1 is represented by positive cosine wave and bit 0 which is represented by -1 is a negative cosine wave and this is created by multiplying the cosine wave with -1. Same process flow is repeated to produce Q phase but this time the sine wave is used to generate the phase. Then, both I and Q phase are added to produce the QPSK signal as shown in Fig. 3.

In the second step, data for each QPSK phase is collect and stored in 4 different Random Access Memory (RAM) blocks. Since all 4 phases for a QPSK is stored in 4 different RAM's, the digital QPSK modulator no longer needed to produce a QPSK phase from I and Q phase as in conventional QPSK modulator. As for simulation

Table 1: Line coded data modulated into I and Q phase

Line coded		Modulated signal	
Even data	Odd data	Q phase	I phase
1	1	-Sin $\omega_c t$	Cos $\omega_c t$
1	-1	-Sin $\omega_c t$	-Cos$\omega_c t$
-1	-1	Sin $\omega_c t$	-Cos$\omega_c t$
-1	1	Sin $\omega_c t$	Cos $\omega_c t$

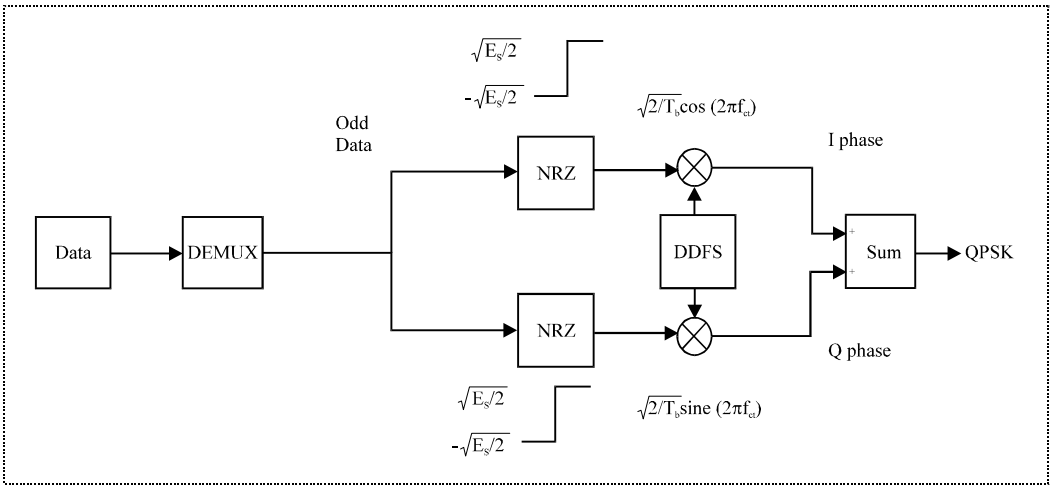

Fig. 2: Conventional digital QPSK modulator block diagram

(a)

	A	B	C	D	E	F	G	H
1						MODULATION		
2	1	0	1	0		SINE PART	COS PART	QPSK
3	SINE	NEG SINE	COS	NEG COS		6	-65534	-65528
4	-6	6	65534	-65534		-4113	-65534	-69647
5	4113	-4113	65534	-65534		-8215	-65534	-73749
6	8215	-8215	65534	-65534		-12286	-65534	-77820
7	12286	-12286	65534	-65534		-16295	-65405	-81700
8	16295	-16295	65405	-65405		-20252	-65017	-85269
9	20252	-20252	65017	-65017		-24118	-64372	-88490
10	24118	-24118	64372	-64372		-27900	-63476	-91376
11	27900	-27900	63476	-63476		-31561	-62326	-93887
12	31561	-31561	62326	-62326		-35108	-60935	-96043
13	35108	-35108	60935	-60935		-38527	-59298	-97825
14	38527	-38527	59298	-59298		-41773	-57434	-99207
15	41773	-41773	57434	-57434		-44864	-55336	-100200
16	44864	-44864	55336	-55336		-47778	-53013	-100791

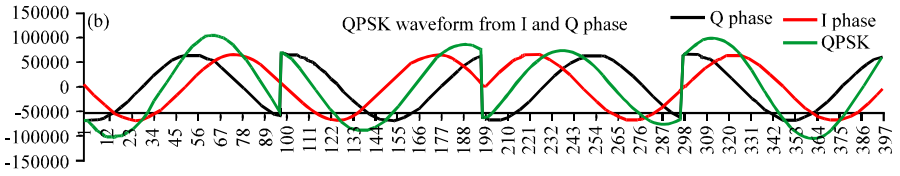

Fig. 3(a-b): QPSK signal generated from I and Q phases

Table 2: QPSK phase data 4 Different RAM's according to input bits

RAM	QPSK phases (degree)	Input bits
1	135	00
2	225	01
3	45	10
4	315	11

purposes, a Pseudorandom Number (PN) sequence generator is used to produce different combination of input. The serial PN sequence will be the input for the 1-2 demultiplexer. The 1-2 demultiplexer will separate the PN sequence into odd and even bits. These odd and even bits will be the input for the 4-1 multiplexer which will select one RAM for different combination of odd and even bits. The input than entered into a 1-2 demultiplexer so that 2 bits of input can choose one RAM's through the 4-1 multiplexer. Table 2 shows the associated RAM's with their QPSK phases and input data.

A Root Raised Cosine (RRC) transmit filter is used to create a pulse shape signal and to up-sample the QPSK waveform (Chattopadhyay and Sanyal, 2010). The RRC filter is crucial in the design since it will minimize the Inter Symbol Interference (ISI) effect at the receiver. The ISI can distort the receive signal and cause error in data interpretation. Equation 2 is used to calculate the bandwidth, B where, f_d represent data frequency and α represent roll of factor. The roll off factor in RRC transmit filter will determine the bandwidth occupied by the transmitted signal:

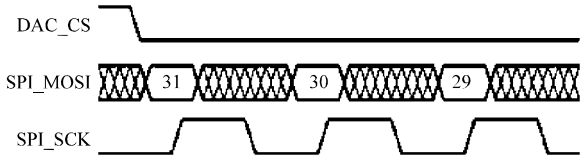

Fig. 4: Timing diagram for SPI communication

$$B = \frac{1}{2} f_d (1+\alpha) \quad (2)$$

The pulse shaped signal is transformed into analog signal using built in Digital to Analog Converter (DAC). The built in DAC with product number, LTC2624 in Spartan 3E board is connected to the FPGA board through the Serial Peripheral Interface (SPI) bus. Figure 4 shows the timing diagram of the SPI communication protocol. Three main signals that are used in SPI communications are, serial peripheral interface master out slave input, (SPI_MOSI), digital to analog converter chip select (DAC_CS) and serial peripheral interface slow clock (SPI_SCK). In this communication process, once the DAC_CS is set to low, the Most Significant Bit (MSB) bits will be transmitted on the SPI_MOSI signal. The LTC2624 capture the signal on the rising edge of SPI_SCK and the data must be valid for at least 4 nsec.

Once all of the 32 bits data has been transmitted, the DAC_CS slave signal is set to high indicating a complete SPI transaction. The LTC2624 supports 24 and 32 bit

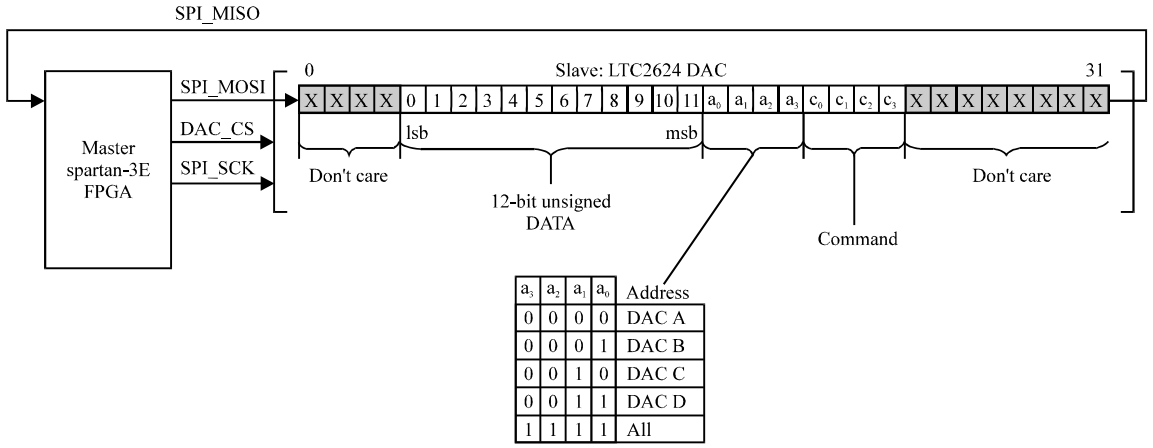

Fig. 5: Communication signal between FPGA and LTC2624 DAC

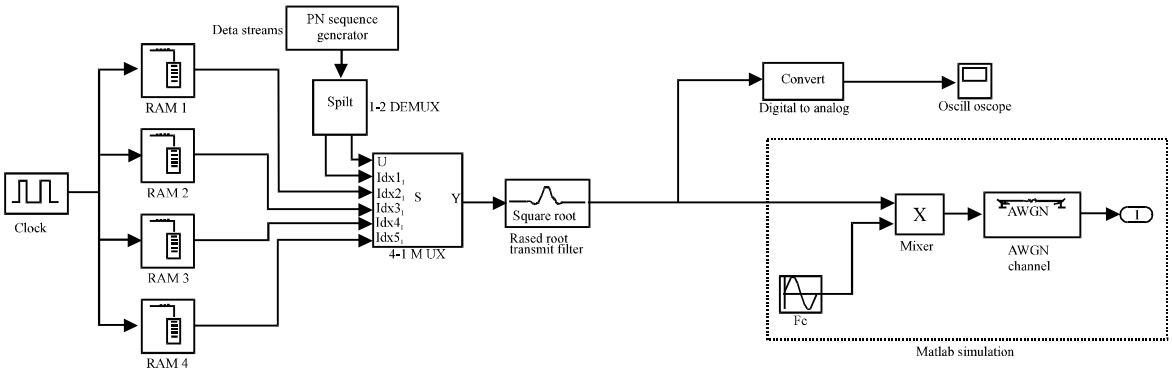

Fig. 6: Complete block diagram for the proposed QPSK modulator

protocol. The 32 bits protocol consists of 8 don't care bits, 4 command bits, 4 address bits, 12 unsigned data bits and 4 don't care bits. For 24-bit protocol, the 8 don't care bits are ignored and the sequence starts with the command bits. A command bit that is used to update the DAC is b0011. The Spartan 3E board has 4 different DAC output ports and address b0000 which referring to DAC A is chosen to update the output voltage. DAC A and DAC B have a reference voltage of 3.3 v while the reference voltage for DAC C and DAC D are 2.5 v. Equation 3 is used to calculate the analog output voltage, V_{out} and Fig. 5 shows the communication signal between FPGA and DAC.

$$V_{out} = \left(\frac{Data[11:0]}{4096}\right) * V_{ref} \quad (3)$$

Following the address bits is the 12 unsigned data bits. This data refers to one data stored in the RAM. This 12 bits value from 0 until 4095 will decide the output voltage level. The modulated data from Spartan 3E board still in low frequency and it need to be up-converted to a higher frequency so that it can be transmitted wirelessly. At MATLAB, a sine wave block act at as up converter frequency and set to 1 MHZ. The frequency later mixed with the modulated signal to produce high frequency signal. The signal then passes through an Additive White Gaussian Noise (AWGN) channel. The AWGN channel will basically add the source signal with some white Gaussian noise to imitate a signal which propagates through wireless atmosphere. By simulating the signal in AWGN channel it will help us on determine the amount of power that we must provide to an input signal before we could transmit it so that it can be demodulated properly. The amount of signal power compare to noise power can be represented with SNR unit and usually defined in decibels scale as in equation 4 where A is voltage Root Mean Square (RMS) of the carrier signals.

$$SNR_{dB} = 20\log\left(\frac{A_{Signal}}{A_{noise}}\right) \quad (4)$$

In practical application, the analog signal output from Spartan 3E board will be up-converted with external RF up-converter according to selected RF band. The propose band is free Industrial, Scientific and Medical (ISM) band which stretch out from 2.4-2.5 GHz. Figure 6 shows the overall block diagram of the hardware implementation using FPGA with a small portion of MATLAB simulation for the modulator.

SIMULATION

The simulation of the QPSK modulator is divided into 2 stages; the first one is to verify the data stored in the RAM is in accordance to the input bits and second is to verify the SPI function for the QPSK data conversion from digital to analog. The ISim simulator provided by the Xilinx is used to run the HDL test bench file written for both behavioral models. The simulator than produce timing diagram for the input and output ports as associated in the test bench file.

DATA EXECUTION

To simulate the data execution, a group of 100 data is stored in one RAM. Data stored in a RAM will be executed according to the input. For example input data 00 will activate RAM 1 to execute data stored inside the RAM. Time taken to execute all data in one RAM is 800 nsec. The SPARTAN 3E board operating frequency is 50 MHZ, the carrier frequency for the simulation is 13 KHz and the speed for the input bits is 3.25 KHz. Figure 7 shows the input bits transition from 1-10 and the time taken for one data execution is 8 nsec.

SPI FOR DAC

The SPI communication for DAC simulation is shown in the timing diagram of Fig. 8. The 24-bit protocol is chosen for the simulation and implementation of this project. The dac_sck signal shows that the dac_mosi signal changes only after 1 clock period which is 8 nsec. This is shown by the yellow and white color label the top of the timing diagram. Other signal is default setup so that FPGA can communicate through SPI with the DAC Integrated Circuit (IC) onboard.

FPGA IMPLEMENTATION

Once the simulation is completed and verified, the behavioral model is developed for FPGA implementation. The HDL behavioral model is synthesized, translated and mapped before a place and route process is done through the Xilinx ISE. Figure 9 shows the full Register Transfer Level (RTL) diagram for the proposed QPSK modulator.

DEMODULATOR IMPLEMENTATION

In order to verify the data transmitted by the modulator, a demodulator is designed using MATLAB

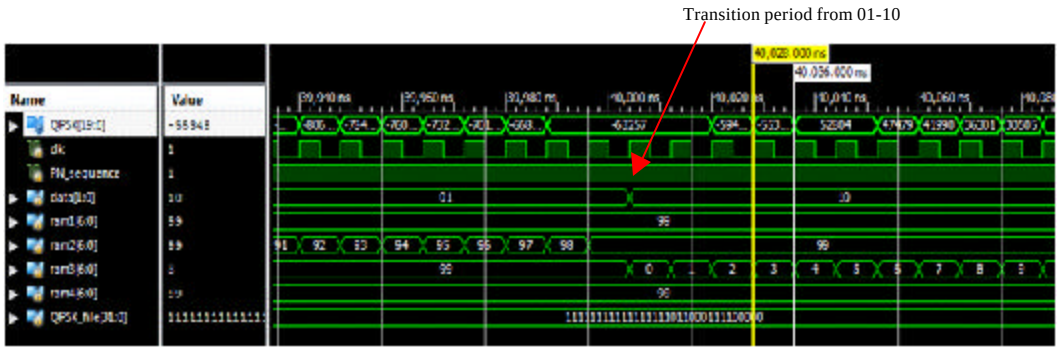

Fig. 7: Timing diagram for QPSK modulator

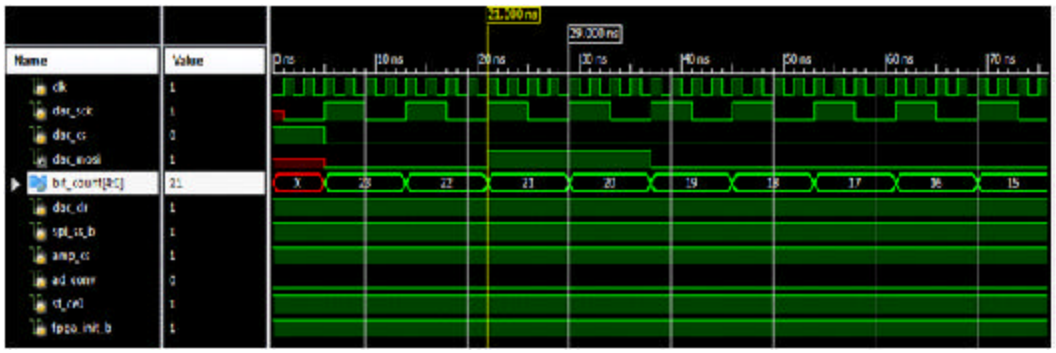

Fig. 8: Timing diagram for DAC

simulink model. The received signal from the modulator is amplified by factor of 2 and down converted to an intermediate frequency with a local oscillator. The local oscillator frequency used is same as the carrier frequency in the modulator which is 1 MHZ. Later, the signal is down sampled and filtered with RRC receive filter. This will produce back the modulated QPSK signal and ready to be demodulated at baseband level.

Demodulation of QPSK signal is a process of mixing the QPSK signal with sine and cosine waveform separately to produce raw even and odd data streams (Chen and Hu, 2008). This method is known as coherent detection method (Burr, 1992). In coherent detection, the carrier has to be recovered from the QPSK signal. A phase locked loop is used to recover the carrier frequency. According to Boerstler (1999) and Langton (2002), the Phase Lock Loop (PLL) detects the incoming frequency by using phase comparison method. Once there is no phase difference in incoming signal and feedback signal, the PLL will lock the output signal to a constant frequency. The PLL output frequency is a cosine waveform and it mixed directly with the QPSK signal to get raw even data. For the raw odd data, the output of the PLL needs to be transformed into sine wave using Hilbert filter. Both of these raw data are then filtered with Low Pass Filter (LPF) and shaped to get back the original even and odd data. Figure 10 shows the complete demodulation process in MATLAB simulink model and Fig. 11 shows the odd and even data retrieved through the demodulation process.

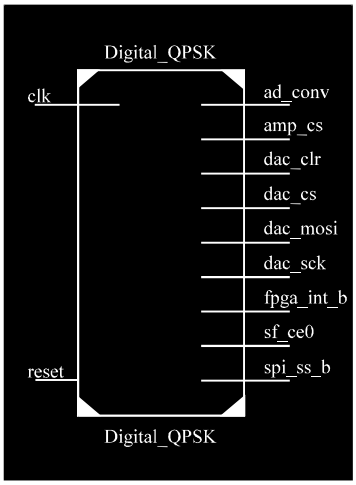

Fig. 9: RTL diagram for the proposed QPSK modulator

POWER ANALYSIS

Xilinx provide 3 types of power analysis tools for three different stages. The XPower Estimator (XPE) tool is usually used in the pre-design and pre-implementation phases of a project. Meanwhile the XPower Analyzer (XPA) tool performs power estimation at post implementation stages. It is the most accurate tool since it can read from the implemented design database the exact logic and routing resources used for a design. The last power analyzer tool provided by Xilinx is PlanAhead RTL power estimator. This software provided an earlier stage of power consumption of a design at RTL level and this is the tools used in this study to estimate the power consumption. Planahead reads the HDL code from a design to estimate the resources needed and reports the estimated power from a statistical analysis of the activity for each resource.

It's clearly shows that the power consumption of the proposed QPSK modulator consumes significantly less than 40% power compared to the conventional

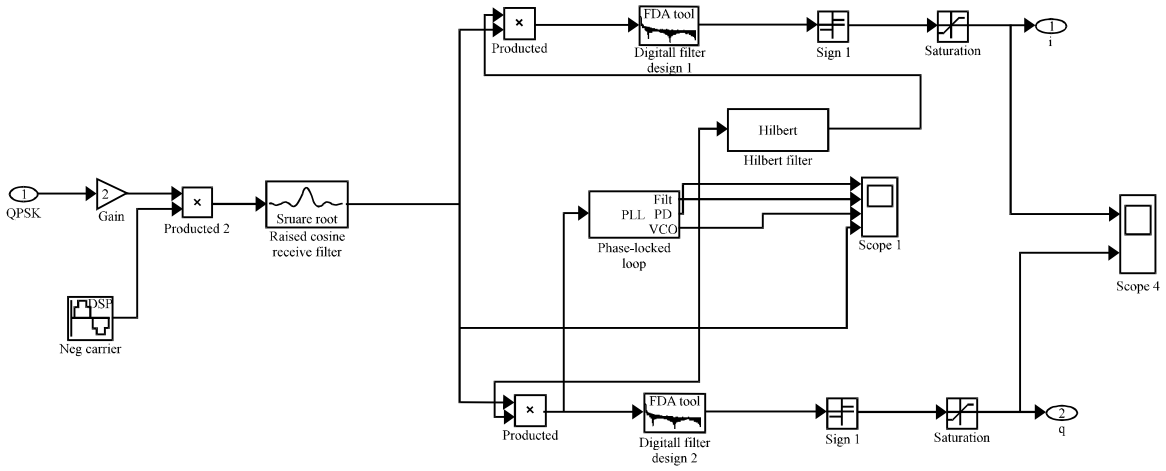

Fig. 10: QPSK demodulation in MATLAB

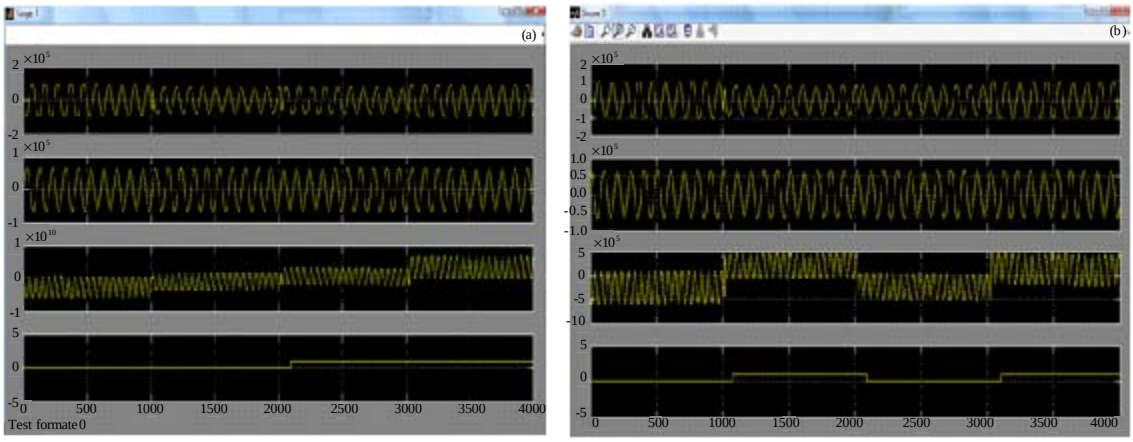

Fig. 11(a-b): QPSK signal, carrier waveform, output of carrier signal mixed with QPSK signal and reconstructed data for even and odd data

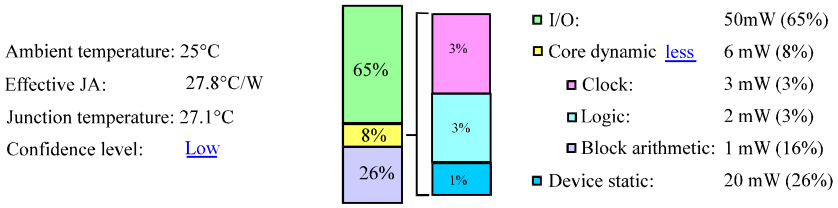

Fig. 12: Estimated power consumption for Conventional QPSK modulator

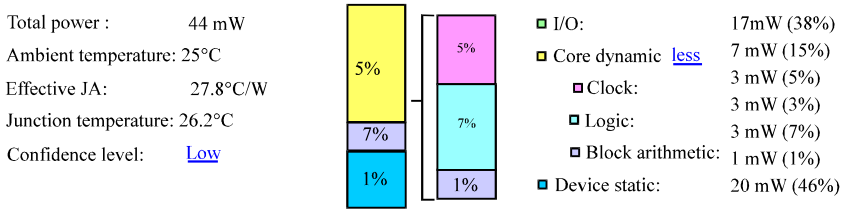

Fig. 13: Estimated power consumption for proposed QPSK modulator

QPSK modulator architecture using the DDS. The results obtained from power tools analysis as shown in Fig. 12 and 13 shows that the conventional QPSK modulator implemented on FPGA consumes total power of 76 mw and while the proposed designed consumed 44 mw, respectively. As can be seen from the Bar chart in details, the I/O power for conventional modulator is 50 mw while for the proposed QPSK modulator is only 17 mw of power. As a result, the proposed architecture consumes significantly less 33 mw less of I/O power and 32 mw in total from the conventional architecture. The reasonable power reduction was mainly because the elimination of DDS which used to generate sine and cosine carrier signal continuously in conventional QPSK modulator.

The device static or also known as leakage power represents the power required for the device to operate and be available for programming consumes almost 26-46% from the overall power consumption for both modulator design. A large portion of it is due to leakage in the transistors used to hold the device configuration. However, according to Kuon and Rose (2006), FPGA consumed more power compare to Application Specific Integrated Circuit (ASIC). The power consumption is high in FPGA due to its flexibility in configuration and rerouting. Therefore significant reduction in power consumption can be achieved once the proposed architecture is implemented in ASIC. Both power analyses were done at ambient temperature of 25°C.

CONCLUSION

The proposed QPSK modulators successfully simulated on Xilinx ISE 12.4 software platform and the results obtain shows the correct functionality of the modulator as with the conventional architecture. While the power analysis tools used to estimate the power consumption on the proposed modulator shows that the proposed architecture consumes less power when compared with the conventional architecture. The power reduction can be achieved due to less usage of input/output logic block in FPGA in conjunction with the elimination of DDS in the new design.

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