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A Novel Low Power Adder-Subtractor using Efficient XOR Gates

V. Elamaran, G. Rajkumar, S. Singh Rajpurohit and R. Anooj Krishnan
Department of ECE, School of EEE, SASTRA University, 613401, India

Abstract: VLSI system and design trend is moving away from speed constraint to power due to the rapid technology evolution growth in the portable consumer electronics market. The operational time of consumer electronic products are highly limited due to limited backup time of batteries. A novel adder-subtractor using XOR gates which are in turn designed with less number of transistors is implemented. Modification of XOR gate portion in a adder-subtractor using minimum number of transistors is the key idea for the design. In future, a study of modification of the entire circuitry involved in the design will be implemented. A comparison of the results with traditional adder-subtractor using conventional CMOS approach using Electronic Design Automation (EDA) tools like DSCH (Digital Schematic) and Microwind layout tools using BSIM4 MOSFET model in 0.12 μm technology is obtained. Results show that all the three approaches are better than a conventional approach by comparing power, speed and layout area.

Key words: Adder-subtractor, IC design, low power, microwind layout tool, XOR gate

INTRODUCTION

Since the transistor count and switching frequency were much low in the past decades, power dissipation was not an issue. As the technology shrinks, plenty of transistors, speedy and become much smaller, are being packed into a chip, which in turn increase the operational frequency and processing capacity per chip at a very higher rate. As a result increased power dissipation has come into picture. Since number of integrated transistors become double in once in 18 months, there is a much need to fabricate low power VLSI chips. Portable consumer electronic products powered by batteries is an another factor for low power VLSI Design, since the battery technology alone cannot solve the low power problem (Yeap, 1998; Vigneswaran *et al*., 2006; Reddy, 2011; Priya *et al*., 2012).

XOR gates are the most fundamental blocks for building adder systems (Haghparast and Navi, 2007). The performance of adder can be improved by designing XOR gate such as using minimum number of transistors but without sacrificing the performance. XOR gates were designed using eight transistors or six transistors in early designs (Leblebici and Kang, 1999). Over the past decade, due to pass transistors concepts, significant improvement has been done with the design of XOR gate using four number of transistors. Radhakrishnan (2001) proposed a formal approach to reduce the number of transistors in XOR and XNOR gates.

An optimized design is much needed at circuit level, which is having minimum transistor count, low energy/power dissipation and enough output voltage swing. A CMOS digital circuit has the total power consumption as:

$$P_{total} = C_{switching}, V_{DD}^{2}, f+f I_{short-circuit}, V_{DD}+I_{leakage}, V_{DD} \quad (1)$$

where, f is the switching frequency, $C_{switching}$ is the charging/discharging capacitance, V_{DD} is the switching voltage, $I_{short-circuit}$ is the short circuit current and $I_{leakage}$ is the leakage (static) current (Vigneswaran *et al*., 2006; Rabaey, 2003; Vigneswaran and Reddy, 2006).

Many larger circuits are almost dependent on adder circuits for their performance. The new improved adder circuits will be much useful in the design of macro cells like arithmetic logic unit, adder-subtractor, high speed multipliers and other digital data processing applications with reduced power. But there is a fundamental trade-off between switching speed and power dissipation. Here the implementation adders which provide less power as well as less area with more speed because of less number of transistors is provided. The necessity for low power digital VLSI circuits may vary from application to application. Due to limited power available in batteries, power reduction must be implemented in devices like mobile phones, personal digital assistants, which is battery operated portable systems (Hu *et al*., 2011; Peiravi *et al*., 2009).

An ultimate aim of designing adder circuits is to reduce the power rather than reducing the delay and area nowadays. Since the number of transistors integrated per unit area are increasing double once in every two years, low power designs could be achieved by adding the complexity in the circuitry. Here the purpose of the study is to design adder with few number of transistors, especially design a novel XOR/XNOR gates to achieve the task.

Corresponding Author: V. Elamaran, Department of ECE, School of EEE, SASTRA University, 613401, India

EFFICIENT XOR GATE AND HALF ADDER DESIGNS

A most efficient XOR gate designs which are implemented using Digital Schematic CAD tool is presented here. Figure 1a shows the six transistor XOR gate which uses pass transistors, transmission gate and an inverter (Brown and Vranesic, 2004). Figure 1b shows that an efficient XOR gate which use only four transistors (Brown and Vranesic, 2004). The second one has nMOS pass transistor, pMOS pass transistor and an inverter. Figure 1c shows that another XOR gate using only three transistors in which the right most transistor should be faster than the other two (Chowdhury *et al*., 2008). So, the third circuit performance depends on the devices sizes like width and length of the transistors involved in the design.

Half adders can be designed using the previous XOR gate design and with a pass transistor to produce carry as a and b. Figure 2 shows the half-adder designs with

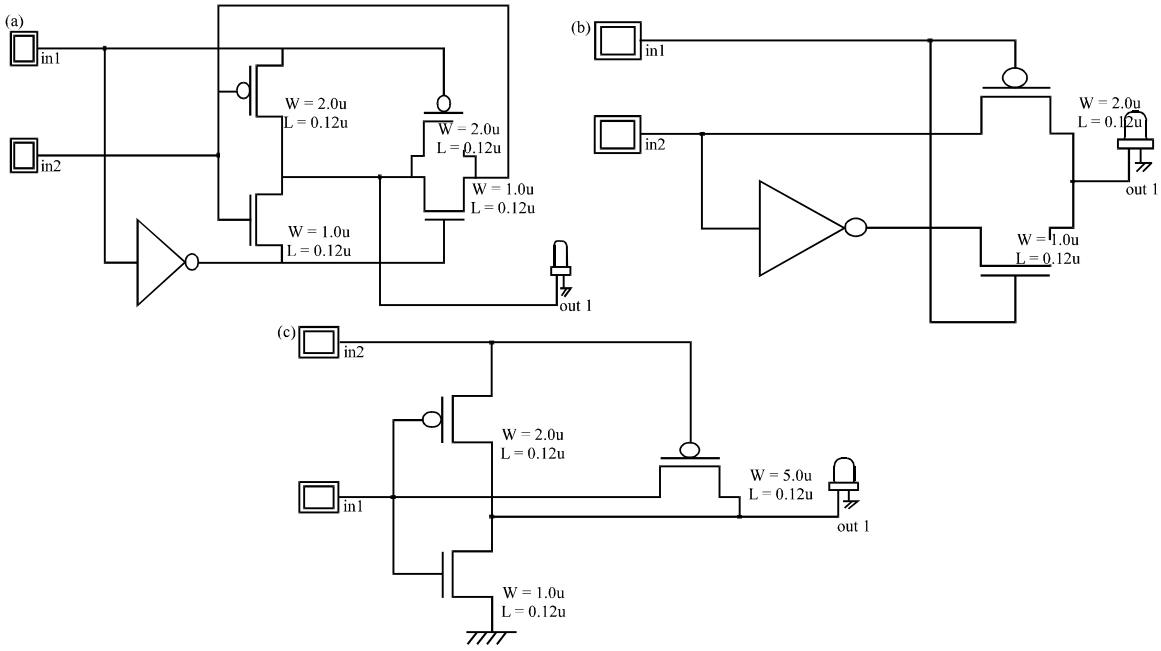

Fig. 1(a-c): XOR Gate using (a) Six transistors (b) Four transistors and (c) Three transistors

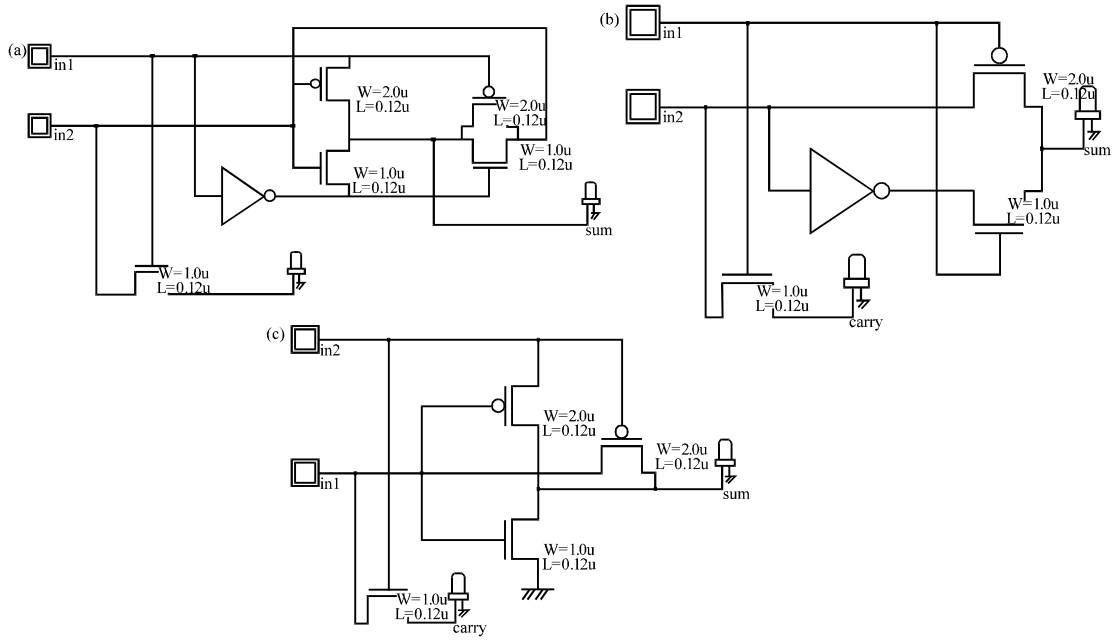

Fig. 2(a-c): Half adder using (a) First XOR gate (b) Second XOR gate and (c) Third XOR gate

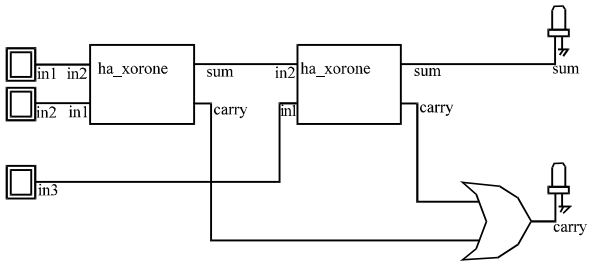

Fig. 3: Full adder using two half adders

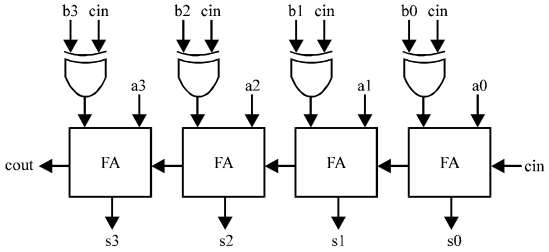

Fig. 4: Adder-Subtractor using XOR gate

corresponding first, second and third XOR gates respectively. A full adder functionality can be verified with Sum and C_{out} and implemented as in Fig. 3.

ADDER-SUBTRACTOR DESIGNS

A more advanced 4-bit adder-subtractor using a 2's complement subtractor can be built by adding XOR gates and an add_sub control it as shown in Fig. 4. The XORs pass the bi bits and the output is the sum (as a+b) when add_sub = 0. The complemented values of bi enter full adders by having control bit of add_sub = 1 which changes the XORs into inverters with carry-in of C_0 = 1. These operations provide (a-b) with 2's complement algorithm (Uyemura, 2002).

A modified design removes one's complement in the first stage at the cost of area and also removes the one half addition is shown is Fig. 5. This design has less area and reduces the critical path delay which helps to enhance the performance of the design. Since half adder is replaced for full adder, it saves more area and removes the need for 1's complement at the cost of area.

The above design is verified using DSCH CAD tool which is a logic editor and simulator used to validate the architecture of the logic circuit. The resulting timing diagram is shown in Fig. 6 using the first XOR gate.

Arithmetic logic circuits play a vital role in systems like microprocessors and other VLSI circuits which evolve even higher levels of performance. In digital processing applications where multiplication and addition is more important, these adder/subtractor units are much useful.

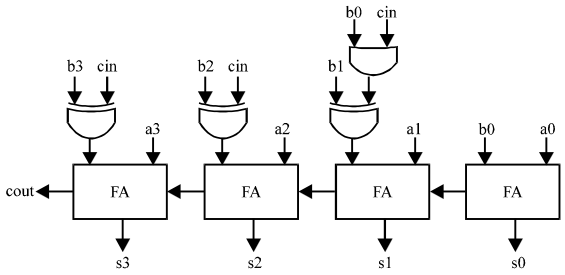

Fig. 5: Modified adder-subtractor using XOR gate

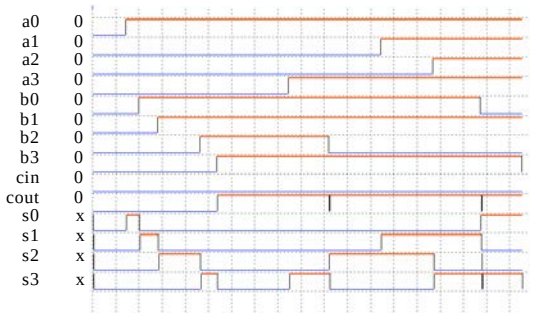

Fig. 6: Timing diagram results

Since at the same time we perform both addition and subtraction, these designs are powerful in many applications.

SIMULATION RESULTS

All simulation layouts presented here are produced by Microwind CAD tool which is a layout editor and simulator. A simulation can be done on the layout produced by the tool. It used mask (MSK) files to store information of the designed layout. Performance characteristics like power dissipation, rise delay, fall delay, layout area and timing diagram results can be provided by this tool.

Since the usage of this tool is very easy, more time spent to have a better design rather than learning how to use the tool. This tool has the facility to convert the layout to Caltech Intermediate Format (CIF) which contains the information for fabrication. Metal Oxide Semiconductor Implementation Service (MOSIS) uses standard masks layout like CIF for fabrication. It has also an EXTRACT program to extract the electrical parameters. A Design Rule Checker (DRC) is invoked and convey the information about any violations of design rule for a particular foundry process.

Figure 7-9 show the layout of 4-bit adder/subtractor using the first, second and third XOR gates, respectively. Figure 10 shows the timing diagram results for the desing using first XOR gate.

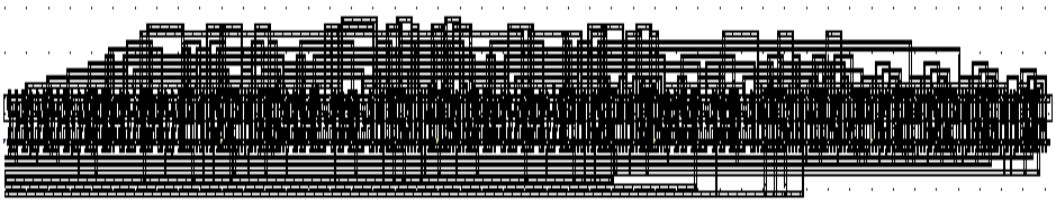

Fig. 7: Layout using first XOR gate

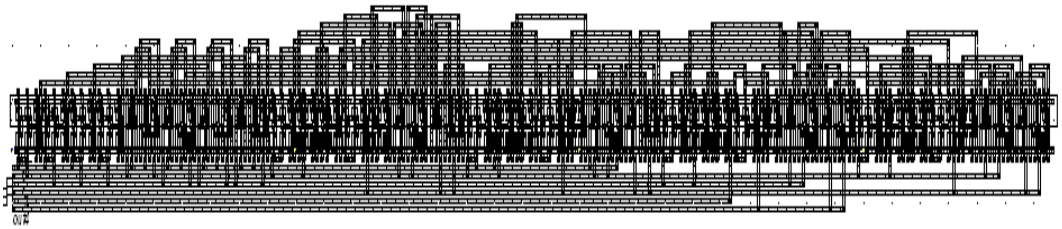

Fig. 8: Layout using second XOR gate

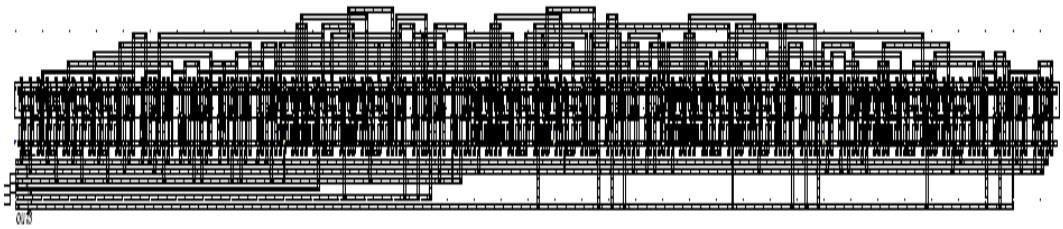

Fig. 9: Layout using third XOR gate

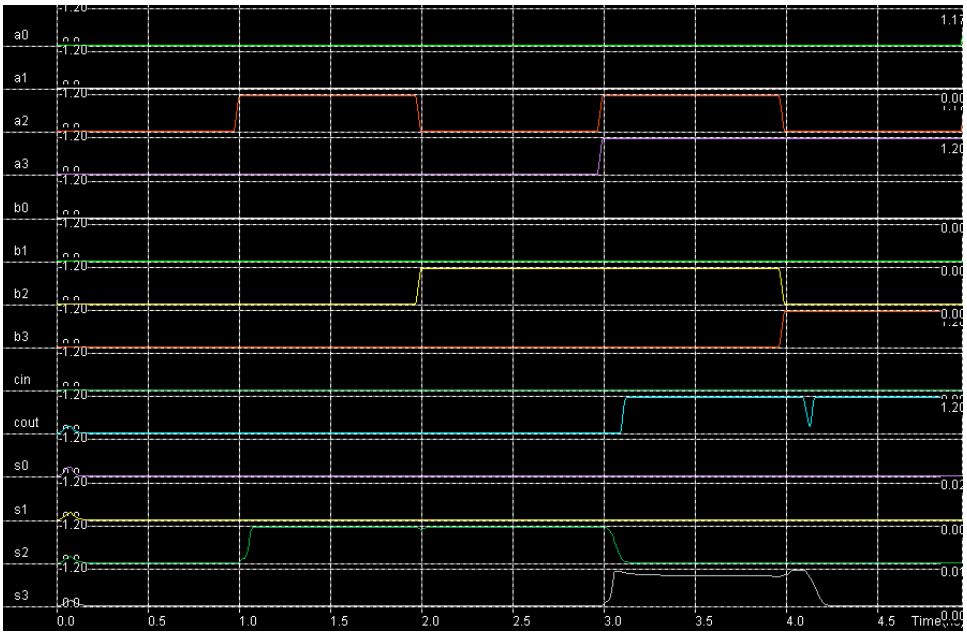

Fig. 10: Timing results on layout

Table 1: Simulation results on layout

Design	Layout area (μm^2)	Power dissipation (μW)
Design using first XOR gate	1701.1	117
Design using second XOR gate	1299.7	188
Design using third XOR gate	1255.8	332
Modified design using first XOR gate	1688.3	109

A simulation is done on the layout for all the designs with VDD = 1.2 V using 0.12 μm process for the period of 20 nsec. Table 1 provide the results of layout area with power dissipation involved in each design.

CONCLUSION

For many processing operations like counting, multiplication, filtering etc., addition forms the foundation. Pass transistors are very powerful for designing such efficient XOR gate which is used in adder circuits. The layout of all the designs are simulated here using Microwind tool. Simulation results show that the design with first XOR gate dissipates less power at the cost of area. The second XOR gate offers low power compared to the third XOR gate with optimum size. Obviously, the third one has less area with more power as expected. The modified design using first XOR gate looks good for low power digital VLSI applications. Here, the simplest and least expensive design that satisfies the specifications should be chosen. Adders are the mostly used blocks in multiplier designs which are much needed for the applications like digital signal processing. In future, this work can be carried out with all the possible of high speed adders.

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