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FPGA Implementation of Audio Enhancement using Xilinx System Generator

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Abstract: Digital audio has become very popular in the last two decades. With the growth of multimedia systems and the World Wide Web, audio processing techniques, such as filtering, equalization, noise suppression, compression, addition of sound effects and synthesis. In this study, an audio enhancement technique using digital FIR filters is implemented. Digital filtering separate signal components based on their frequency content. So that signal can be enhanced with certain or desired frequency components using band pass digital filter. This approach is designed using Simulink and Xilinx DSP Tools, synthesized with ISE 13.2 and implemented on Virtex4 xc4vsx55-12ff1148 FPGA device. Results show the resource utilization on device using bandstop FIR filter designed by Equiripple technique.

Key words: Digital audio processing, FIR filter, FPGA implementation, Xilinx system generator

INTRODUCTION

Audio engineering encompasses the recording, storage, transmission and reproduction of signals to which people listen. In practice, such signals are predominantly natural music, although such signals are electronics music, bird calls, theatrical performances and underwater sounds must be also included. Unlike digitally processed speech which must be subjected to an intelligibility test, much digitized audio is required to meet fidelity criteria as well (Mandal, 2002). In an audio storage and transmission system, the quality of the signal may degrade due to various reasons. For example, a low quality speech production system would produce a poor quality audio. The presence of background noise introduced during audio compression is another source of degradation. Audio enhancement algorithms can be used to reduce the noise contained in a signal and improve the quality of the audio signal. In this study, digital filtering technique is presented. If the noise component in a signal has a narrow spectrum, a straightforward digital filtering can be applied to suppress the noise components (Ownby and Mahmoud, 2003; Singh *et al*., 2012).

Field Programmable Gate Arrays (FPGAs) are digital integrated circuits which can be reconfigured using hardware description languages to specify certain designs and functions. The development of FPGAs started up in the late 1980's and has grown rapidly ever since.

Simulink is a programming environment tool within MATLAB which is commonly used for modeling, simulating and analyzing complex signal processing systems. Its advantage over the regular MATLAB programming environment is that systems are built and tested using customizable graphic blocks.

System Generator (Xilinx Corp, 2001; Moreo *et al*., 2005; Elamaran and Rajkumar, 2012) was developed by Xilinx, an FPGA development company. It integrates the graphical capabilities of Simulink in order to easily bring forth block diagrams to download to FPGAs. It provides a user the ability to (1) Develop and test a software simulation of an FPGA implementation within the Simulink environment, (2) Then convert the simulation FPGA design code (VHDL/Verilog), download this code onto FPGA residing on a development board and run/test the implementation on an FPGA using Simulink inputs and outputs and (3) Then run the FPGA implementation using the input/output capabilities of the development board. These three development steps are called, respectively, software simulation, hardware co-simulation and hardware implementation. The System Generator environment provides a relatively simple and flexible environment for developing FPGA applications compared to VHDL or Verilog hardware description languages. In this study, author's develop a simple band stop FIR filter (Mitra, 2001; Vigneswaran and Reddy, 2007) using Equiripple method to filter the noise component from an audio signal. This work produce results which are implemented on a Xilinx FPGA Virtex4 xc4vs55 -12 ff1148 target device with discussions.

An ultimate aim of this work is to analyze the signal in the frequency domain and to implement filtering according to the spectrum result with the help of

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MATLAB and Xilinx System Generator. An experience working with Xilinx FPGA tools helps a lot in both signal processing domain as well as in the Very Large Scale Integration (VLSI) domain. Integration of Xilinx tools with MATLAB environment is an another objective to simplify the task rather than writing Hardware Description Language (HDL) codes.

FILTER DESIGN SPECFICATIONS

Even though we represent signals and waveforms mostly in the time domain, the frequency domain helps a lot to understand more about the signals rather than the time domain. The presence of signal's energy as a function of frequency is displayed by the spectral domain; in other words, for each frequency value, the frequency-domain representation displays the amplitude (amplitude spectrum) and phase (phase spectrum) of the signal. Frequency domain does not show additional information for signals like sine or cosine but very useful for the signals like an audio signal. So, that the occurrence of noise and original sound can be displayed in terms of frequency which is much useful for designers to choose a cut-off frequency for the selection of signals.

Figure 1 depict the time-domain and power spectral density of a noisy audio signal. The power spectral density shows that the signal has frequency components across the entire 0-24000 Hz range. It is observed that the signal has a noise at 2 kHz frequency which will be eliminated by a band stop filter. A band stop 50 tap FIR filter is designed using Filter Design Analysis Tool with sampling frequency of 48000 Hz (Mitra, 2001; Openheim, 1978; Manikandan and Madheswaran, 2007). These FIR filter coefficients can be exported to the workspace and then will be used by Xilinx System Generator FDA Tool. To implement such a real-time audio signal processing applications on FPGA target device using XSG is the main objective of this study.

SYSTEM GENERATOR DESIGN BLOCKS

Simulink and Xilinx ISE tool: MATLAB/Simulink is a tool which is a pertinent software package for DSP algorithm developments. Algorithms are implemented in FPGA hardware devices using Xilinx ISE tool. Xilinx system generator can be used as a best choice to implement DSP algorithms in a hardware by filling the gap between MATLAB/Simulink and Xilinx ISE tools (Elamaran *et al*., 2012).

Xilinx system generator tool: FIR filter coefficients are evaluated using the Filter Design and Analysis Tool (FDA) from MATLAB software package. The FDA Tool is invoked to specify the filter order and coefficients and the Xilinx FIR compiler Blockset is used for the implementation in Simulink simulation. The algorithms/system can be verified using MATLAB Simulink blocks. Xilinx System Generator is part of Simulink tool box. System Generator is used to generate VHDL/Verilog and all supporting files. Xilinx ISE tool is used to synthesize, implement and programming of FPGA.

Implementation using XSG tool: By using FDA Tool, FIR filter is designed with:

- Sampling frequency (Fs): 48000 Hz
- Response type-bandstop
- Type of filter-equiripple FIR

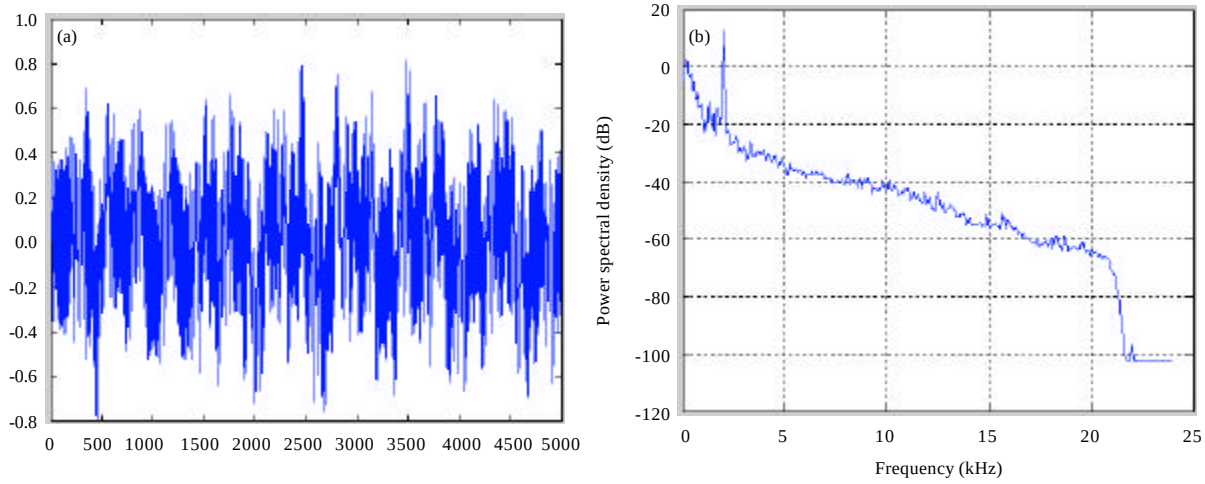

Fig. 1(a-b): Noisy audio signal in (a) Time domain and (b) Power spectral density

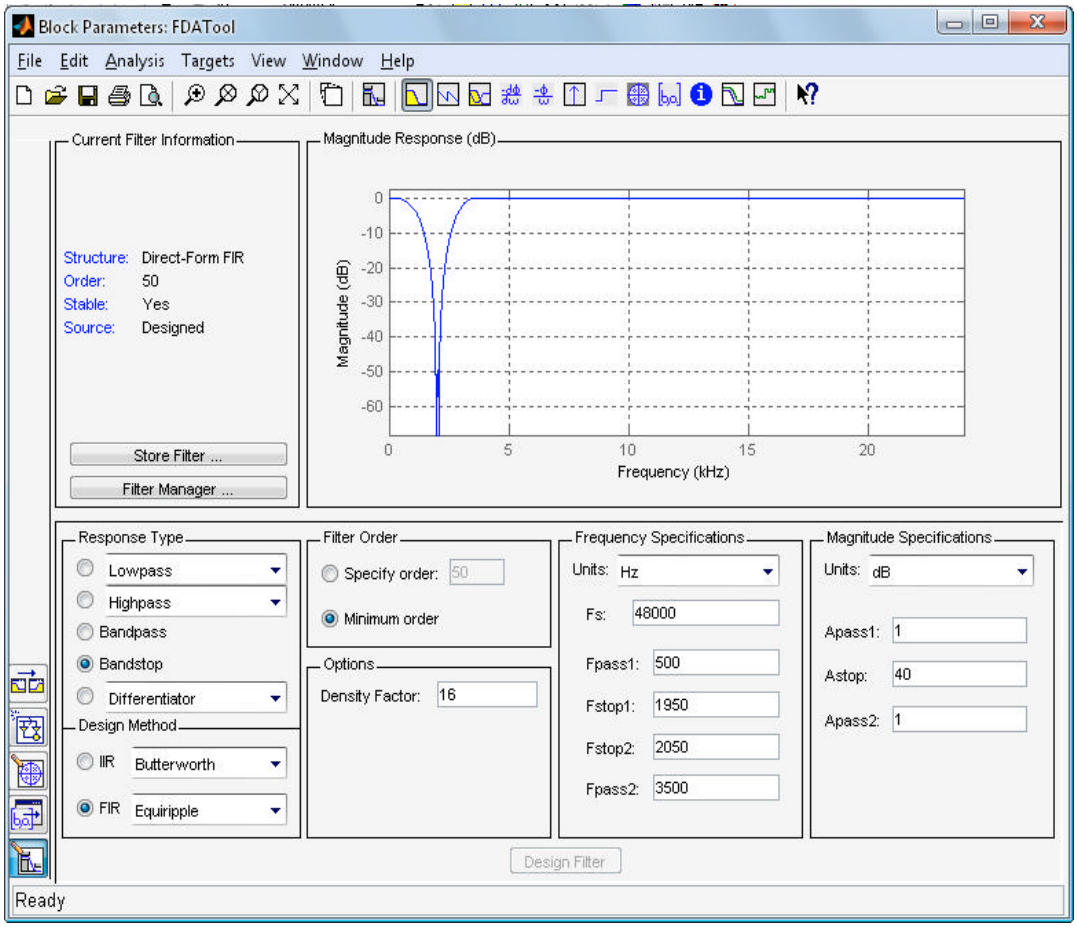

Fig. 2: FDA tool specifications

- Fpass: 1-500 Hz
- Fstop: 1-1950 Hz
- Fstop: 2-2050 Hz
- Fpass: 2-3500 Hz
- Order: 50
- Pass band1 attenuation: 1 dB
- Stop band attenuation: 40 dB
- Passband 2 attenuation: 1 dB

These details are implemented as shown in Fig. 2. An implementation of this using Xilinx system generator is shown in Fig. 3.

The Xilinx FIR Compiler 5.0 block does a Multiply Accumulate (MAC) based FIR filter. A sequence of input data is applied and the filtered output is computed with a fixed delay, based on the filter configuration. Filter coefficients which are computed using FDA Tool are used in FIR Compiler 5.0 block.

Figure 4 shows the set up for system generator token for the target device Virtex 4 xc4vsx55 -12 ff1148 and uses VHDL as a hardware description language (Venkateswari and Muthaiah, 2012). Traditionally, FPGAs are configured with text-based VHDL or Verilog hardware description languages. This provides access to all the FPGA's resources and allows functions to be optimized right down to the last detail. Virtex family target FPGAs have sophisticated blocks like fast adders, multipliers and flexible memory architectures in the logic fabric. For the case of ALTERA based FPGA target devices, DSP Builder tool can be used for the similar task. Signal compiler may be used here, instead of system generator token.

SIMULATION RESULTS

The time domain representation of both the noisy audio and noiseless audio waveforms are shown in

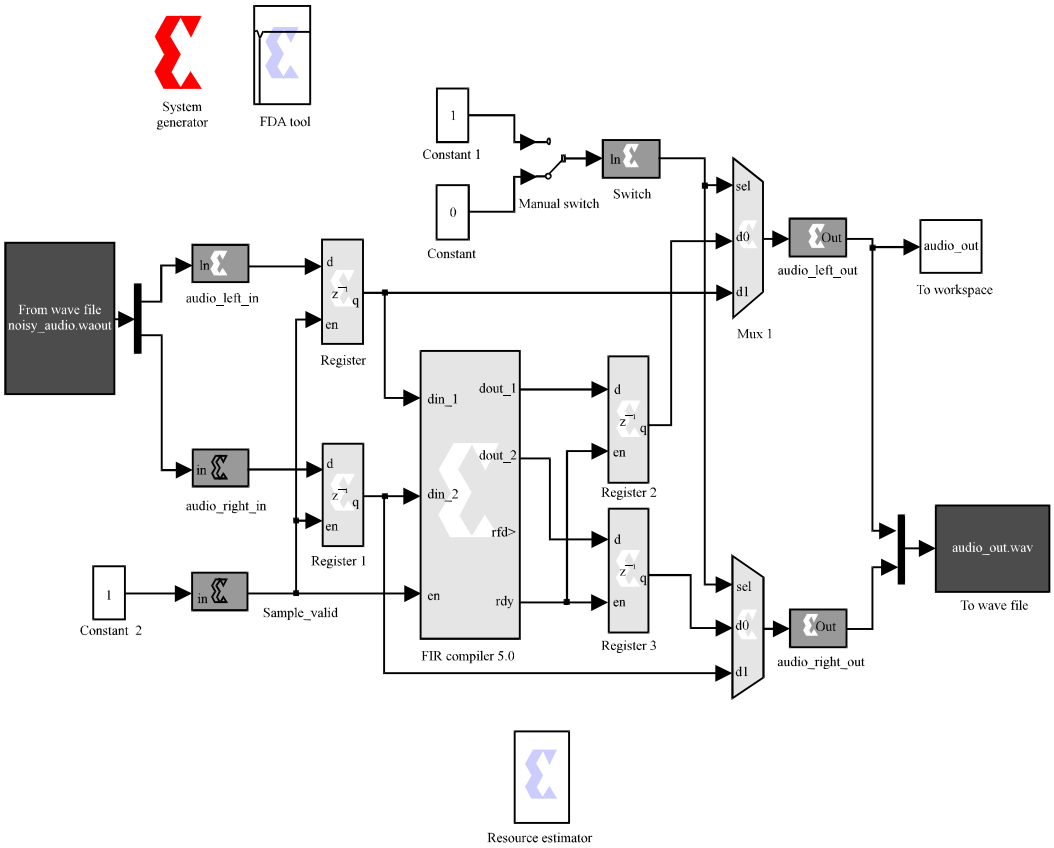

Fig. 3: Band stop filter implementation

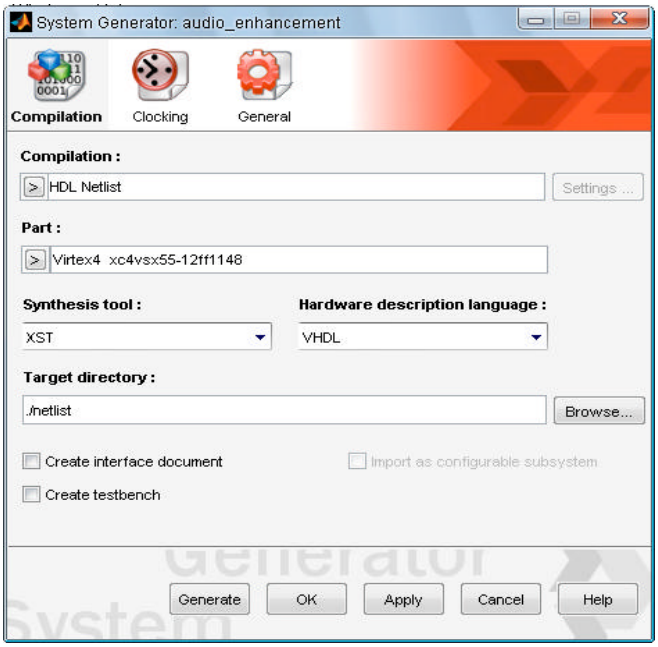

Fig. 4: System generator token

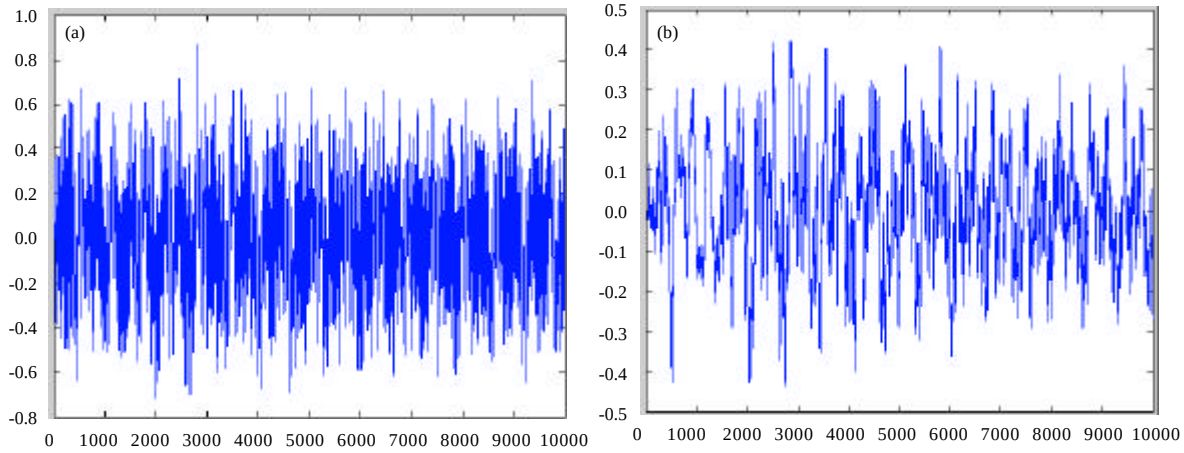

Fig. 5(a-b): Audio in time domain (a) Noisy input and (b) Noiseless output

Table 1: Report of device logic resources usage

Device utilization summary

Logic utilization	Used	Available	Utilization (%)
Logic slices	2,231	24,576	9
Flip-flops	2,612	49,152	5
4 input LUTs	3,364	49,152	6
IOBs	100	640	15
DSP 48 (sec)	52	512	10

Fig. 5a, b. To estimate the resources used in FPGA quickly, the Xilinx Resource Estimator block can be used.

Timing report: The timing summary has been shown as:

- Speed grade: -12
- Logic delay: 3.255 nsec (92.4% logic)
- Routing delay: 0.266 nsec (7.6% route)
- Total delay: 3.521 nsec

Resource utilization report: The area utilization of the implemented design has been shown in Table 1.

CONCLUSION AND FUTURE WORK

Since, the time to design a system is very less, XSG plays a vital role for prototyping a design on FPGAs in the industry. Since, doing DSP concepts and FPGA implementations are possible, this tool could be mostly wanted for the designers and programmers. Like audio, images can be processed and filtered like point processes, area processes and frame processes, etc. Using simple example, we have demonstrated audio enhancement technique which can be extended by using spectral subtraction, Wiener filtering and adaptive noise cancellation techniques.

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