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The Structural and Electrical Studies of TiO_2 Thin Films Grown by Sol-gel Spin Coating Technique

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ABSTRACT

Recently much research has been reported that a transparent oxide semiconductor having optical band gap wider than 3 eV can be applied in microelectronics applications. The TiO_2 is the one which meets this requirement. So TiO_2 thin films have been deposited on well clean P-type silicon substrates via a sol-gel spin coating method. The phase structure and morphologies of thin Nano crystalline film were characterized by X-Ray powder diffraction (XRD), Field-emission Scanning Electron Microscope (FESEM) and Atomic Force electron Microscope (AFM). The structural characteristics carried out for as deposited thin films shows amorphous nature. The crystallite sizes of the TiO_2 particle measured from the typical diffraction peaks and found to be approximately 38 to 65 nm. The annealed films were found to be Nanocrystalline in nature and also greatly improved at higher temperature in N_2 atmosphere. The Raman spectra peaks were observed at 144, 192, 390 cm, 519 and 634 cm^{-1} for active anatase phase of TiO_2. The electrical properties were investigated by capacitance-voltage (C-V) and current-voltage (I-V) analysis. The dielectric constant 27 and optical dielectric constant 5.43 were found by C-V analysis and ellipsometry respectively. This paper investigates the sol-gel process to deposit Nanocrystalline TiO_2 thin films with simple and cost effective experimental set up.

Key words: SEM, XRD, Sol-Gel spin coating method, nanocrystalline film

INTRODUCTION

Wide band gap semiconductor material are being of special interest for today research due to their potential application in various fields, such as sensors, LEDs, laser diodes, photovoltaic cells and high speed devices (Ivan *et al*., 2009; Chong *et al*., 2006). TiO_2 thin films can be applied in microelectronics (Sun *et al*., 2010), optical cells, solar energy conversion (Fuyuki and Matsunami, 1986), highly efficient catalyst (Shockley, 2005) and gate oxide in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) (Springer Publishers, 2007). Optical properties of TiO_2 include wide electron energy band gap, transparency through visible spectrum and high refractive index from the ultraviolet to far infrared spectral range. The outstanding properties and chemical stability in hostile environment attracts its study (Masuda *et al*., 2002). Many sophisticated fabrication techniques namely, vacuum evaporation (Lobl *et al*., 1994), molecular beam epitaxial (Georgia *et al*., 2006), chemical vapor deposition (Battiston *et al*., 1994), laser-assisted vacuum evaporation (Lobl *et al*., 1996), various sputtering methods, reactive Direct Current (DC) or Radio Frequency (RF) magnetron sputtering (Meng and dos Santos, 1993), ion beam techniques

(Martin *et al.*, 1996) are used for fabrication of thin films. However these techniques have several shortcomings, such as expensive vacuum equipments, need to heat the substrate to crystallize the films and limitations of line-of-sight deposition (Liu *et al.*, 2003). In practice for upcoming ULSI technologies (0.32 nm and beyond), require an arbitrarily high-κ dielectrics material to scale down the gate oxide thickness. The leakage current increase exponentially when gate oxide reduced below 3 nm (Wilk *et al.*, 2001). The attempt to reduce the leakage current is the main driving force behind the switch to the high-κ dielectric material. So the alternate gate dielectrics with high dielectric constant are being currently investigated for next generation MOS technology (Wong and Iwai, 2006). The high dielectric constant of these films makes them useful for the MOS capacitor structure grown on Si substrate. The as deposited films using sol gel process have been characterized by X-Ray diffraction for composition. Capacitance-Voltage (C-V) and current voltage (I-V) have been used to determine the interfacial and electrical properties of the MOS capacitor.

MATERIALS AND METHODS

The film of TiO_2 has been deposited on the silicon (Si) P substrate having crystal structure <100> using sol-gel method. NMOS capacitors were fabricated on P-100 Si substrates with boron background doping of approximately 5×10^{15} cm^{-3}. The wafer size was 3 inch and was cut in to 2 and 3 pieces. After this wafers were cleaned using a standard RCA clean method to prepare the surface for dielectric deposition. The sol was prepared by mixing TIP with absolute ethanol and acetic acid in the molar ratio of 1:8:0.1. In order to control the reaction kinetics acetic acid was used as the chemical additive to moderate the reaction rate. The water used for hydrolysis in solution was added gradually under magnetic stirring. The molar ratio of the reactants was 1 mole of TIP (Ti (i-$C_3H_7O_2)_4$) of 99.9% purity is mixed with 8 mole of ethanol absolute grade. TIP was hydrolyzed by slow addition of cold water and 0.1 mole of acetic acid added to catalyzed the hydrolysis. The final mixture was maintained under magnetic agitation at 85°C for 45 min.

To obtain the film, the substrate was placed on spinner (home-made) and drops of the above mentioned solution were placed on the substrate. The substrate was then allowed to spin for 1 min with spinning rate of 2000 rpm. The sample was removed from spinner and baked for 20 min at 95°C. Successive spin coating cycle (sol-gel deposition plus heat treatment) of the substrate was carried out in the sol-mixture. After each spin coating cycle, the film is annealed in the dynamic air at 550°C for 30 min. In order to treat the adsorbed films thermally, the wafer were put in a temperature controlled tube furnace.

The aluminum metal was deposited by thermal evaporation using a physical mask to make dots on front side of the TiO_2 film and at the back of the Semi conductor to from Si/TiO_2/Al structure for C-V analysis. Figure 1 shows the experimental set up of the chemical process.

Film characterization: The thickness 52 nm of the as deposited film was measured using stylus profiler. The grain size as well as crystalline phase of TiO_2 has been determined using an X-Ray diffractometer. The target was consisting of copper metal where ac nickel metal is used as β-filter. To determine various peaks obtained in XRD spectrum Joint Committee powder Diffraction Standards (JCDPS) files were used. The C-V (capacitance-voltage) curve was obtained using C-V analyzer (Keithley 590). Capacitance curves were measured from -4 V to +4 V. SEM micrograph were obtained using JEM-1200 Ex (JEOL) model. The accelerating voltage was kept at 15 kV and tube current was 10 mA. The Aluminum (Al) metal was deposited by the thermal evaporation system on the back side of the sample for the ohmic contact. A physical mask was used to make

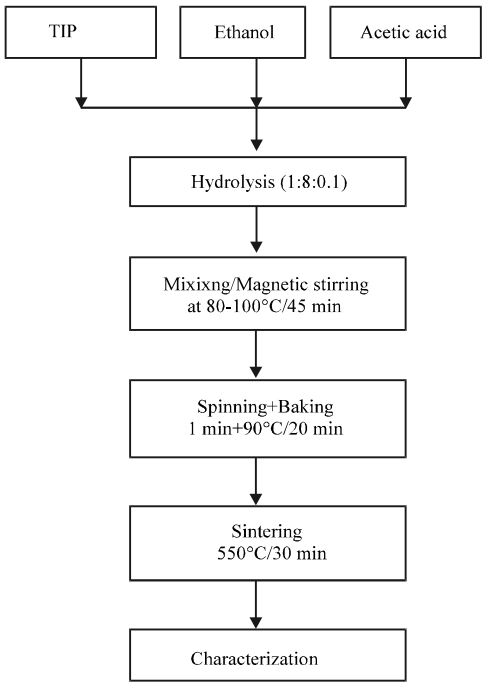

Fig. 1: Experimental setup

dots on the front side of TiO_2 film. Before the deposition of dot, samples were annealed in vacuum at 300°C for good ohmic contact. In this work, we report on the characteristics of TiO_2 dielectrics with respect to Equivalent Oxide Thickness (EOT), flatband voltage V_{FB}, leakage, work function and thermal stability.

RESULTS

Thickness composition and structure: A surface profiler was used to measure the as deposited thickness of TiO_2 thin film and found to be 52 nm. The crystalline phases were detected and identified by X-ray Diffraction (XRD) pattern for as-deposited and annealed (550°C for 30 min in ambient air and 850°C in N_2) TiO_2 film. The grain size was calculated by the Scherer's formula $D = 0.89\lambda/\beta_{1/2}Cos\theta$, where λ is X-ray wavelength, $\beta_{1/2}$ is Full Width at Half Maximum (FWHM) of diffractions line and θ is diffraction angle. The XRD exhibits different crystalline phases of TiO_2 thin film and calculated grain size of TiO_2 (004), (200) and (211) phases are 38, 47 and 65 nm, respectively. Figure 2 shows the XRD pattern of TiO_2 film deposited at Si wafer and annealed at 550°C in air and 850°C in nitrogen ambient as shown in Fig. 2a and b, respectively. The XRD exhibit the peaks of crystalline phase and grain size of TiO_2 thin films increases with annealing and calculated grain size of TiO_2 (004), TiO_2 (200), TiO_2 (211) was 71, 69 and 63 nm, respectively. The XRD patterns also confirm that the TiO_2 thin films deposited under ambient conditions are amorphous and the films annealed at different temperatures are polycrystalline with a tetragonal structure.

In Fig. 3, the porous nature of the film is clearly visible when annealed at 550°C, also supports that surface is smooth and compact. The AFM images were subjected to flattering process. Then according to quantitative analysis measured value of average roughness (R_a), Root Mean Square (RMS) value and coefficients of kurtosis (R_{KU}) were 0.31, 0.40 and 0.76 nm, respectively at 550°C.

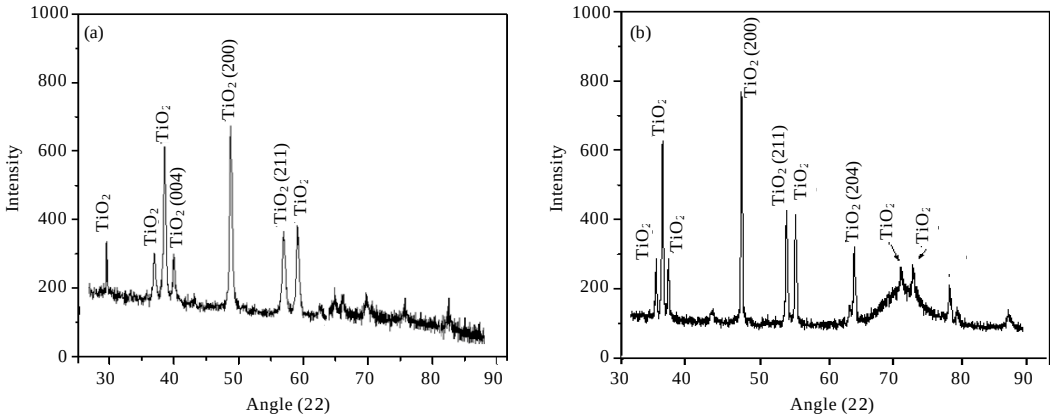

Fig. 2(a-b): (a) XRD pattern of TiO_2 film deposited on silicon wafer annealed at 550°C (b) XRD spectrum of the titanium oxide film annealed at 850°C

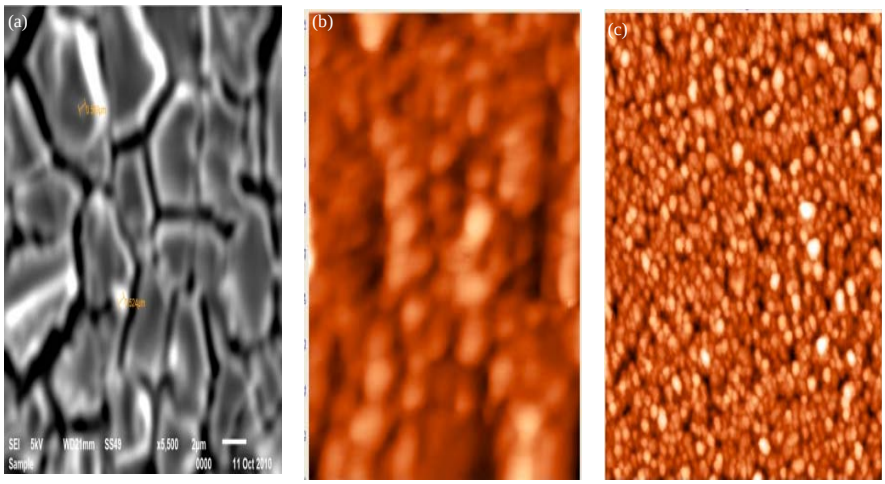

Fig. 3(a-c): (a) SEM picture of TiO_2 annealed at 550°C, AFM images of scan area of 1 μM×1 μM annealed at (b) 550°C and (c) 850°C

The literature clearly states that 0.1 nm oxide, a 0.1 increase in the Root-mean-square (RMS) interface roughness can lead to 10 fold increase in gate leakage current. The film is composed of randomly oriented grains and the size affected with annealing temperature as shown in Fig. 3b and c. The increase in annealing temperature reveled that increase in mean size of grains and reduces the grain boundary area. This happens due to migration of smaller crystallites and joining with bigger crystallites with same orientations. This statement agrees with the result of XRD in Fig. 2a and b as well as in Fig. 3b and c.

The Raman spectra of spin coated TiO_2 thin film annealed at 550°C is shown in Fig. 4. The result of XRD spectrum was endorsed by Raman spectra. The three raman peaks at 144, 192 and 634 cm^{-1} are aggined to the E_g mode of Anatase phase, which supports the result of literature. The peak at 390 cm^{-1} was obtained corresponding to B_{1g} mode and 519 cm^{-1} for the A_{1g} and B_{1g} modes.

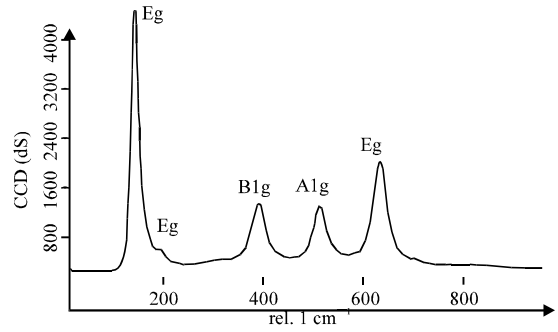

Fig. 4: Raman spectrum of TiO_2 thin film annealed at 550°C

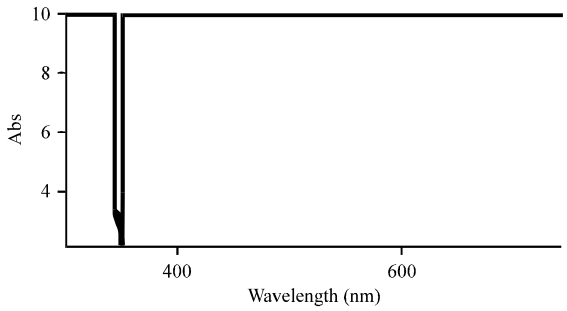

Fig. 5: The absorption spectra of TiO_2 thin film

So TiO_2 have six Raman active modes $A_{1g}+2B_{1g}+3E_g$. The absence of peaks corresponding to Rutile phase confirms the only Anatase active mode of TiO_2 films supports the value reported elsewhere (Ohsaka *et al.*, 1978). Although the absence of overlapping peaks strengthen the well crystallinity of the films but roughness of 0.3 nm was observed by AFM flattering analysis.

Electrical and optical properties: The refractive index of the TiO_2 film measured by ellipsometry was found to be 2.33 and optical dielectric constant can be determined from the refractive index of TiO_2 $\epsilon opt = \epsilon_0^2 = 2.33^2 = 5.4389$. The band gap was calculated 3.6 eV by using equation $\epsilon = hc/\lambda$, ϵ is photon energy, c speed of light and λ cut of wavelength by the help of Spectrophotometer as shown in Fig. 5.

Capacitance-voltage analysis: The samples were characterized by C-V Keithley 590 CV analyzer, 595 Quasi static CV-Meter and 230 Voltage Source connected with remote input output coupler. The fabricated capacitor electrically tested to characterize the material and to inspect the device performance. Figure 6 shows the variation of the capacitance with gate voltage (V_G) ranging from -4 volts to +4 volts at 100 kHz frequency. C_{ox} is oxide capacitance measured by C-V curve for Accumulation region = 56 pF from Fig. 6. While in the inversion region, where the total capacitance per unit area ($C_{a,min}$) is the series combination of the oxide capacitance and the steady minimum depletion capacitance. The inversion capacitance per unit area is given by equation:

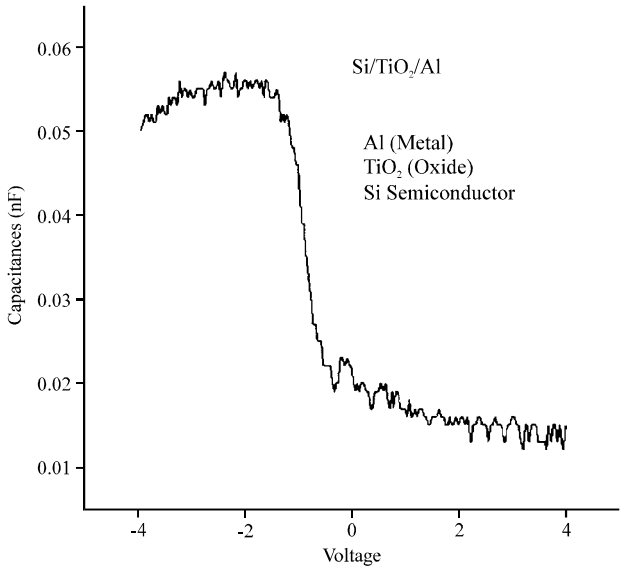

Fig. 6: CV Characteristics of Si/TiO_2/Al structure

$$C_{a,min} = \left[\frac{1}{C_{ox}} + \left(\sqrt{\frac{q \in_{si} N_d}{2(2\varphi)}} \right)^{-1} \right]^{-1}$$

and:

$$\varphi = \frac{kt}{q} \ln \left(\frac{N_d}{n_i} \right)$$

where, C_{ox} oxide capacitance, electronic charge, $\in_{si}$ is the permittivity of the substrate = $11.7 \times 8.85 \times 10^{-14}$, N_D is density of carrier concentration in the doped substrate, n_i is carrier concentration in intrinsic semiconductor. Now the flat band capacitance given as:

$$C_{FB} = \frac{\frac{C_{ox} \in_s A}{(1 \times 10^{-12})(\lambda)}}{(1 \times 10^{-12})(C_{ox}) + \frac{\in_s A}{(1 \times 10^{-12})(\lambda)}}$$

where, λ is the extrinsic Debye length, as calculated:

$$\lambda_D = \sqrt{\left(\frac{\in_s kT}{q^2 Nx} \right)}$$

where kT is thermal energy at room temperature. Debye length indicates that how far an electrical event can be sensed with in the semiconductor. The flat band capacitance C_{FB} = 51.77 pF, C_{OX} is

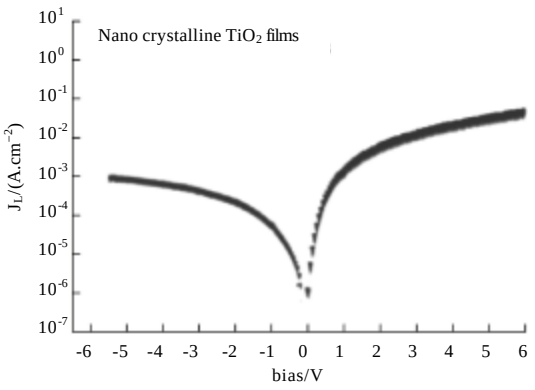

Fig. 7: Gate leakage current vs. electric field

the oxide capacitance = 56 pF and A is gate area = 3.13×10^{-6} .This C_{FB} is less than the $C_{A,MIN}$ = 59.5 pF. By the C-V characteristics of the capacitor the flat band voltage V_{FB} of the capacitor can be estimated. Now the threshold voltage V_{TH} for MOS-C from a C-V curve as follows:

$$V_{TH} = \left[\frac{A}{C_{ox}}\sqrt{4E_s qN_{BULK}\varphi_B} + 2\varphi_b\right] + V_{FB}$$

where V_{TH} calculated was -0.329 V. The dielectric constant (k) calculated from the knowledge of the capacitance (C_{ox}) using C-V curve was found to be 27. The physical thickness of alternative high-κ dielectric employed to achieve the equivalent capacitance density can be obtained from the expression $T_{high\text{-}k} = (K_{high\text{-}k}/Kox)Teq$. The increasing thickness of dielectric impacts on tunneling current. The interface trap density (D_{it}) was calculated using relation (1×10^{-12}) C_{it}/Aq here C_{it} is the interface state capacitance. The value of interface trap density was found to be $(1.1\times10^{12})cm^{-2}eV^{-1}$ and oxide charge density was $8.9\times10^{12}\,cm^{-2}$, which were slightly higher than reported values. The electrical properties of TiO_2 films as the gate bias were also investigated. It can be noted that the as deposited film showed a relatively low leakage current (J_L) of about 10^{-6} A/cm^2 at zero bias and 5.32×10^{5} A/cm^2 at a gate bias of +1 V (Fig. 7).

DISCUSSION

Titanium dioxide films having well crystallized Anatase phase confirmed by XRD and spectrophotometer. Grain sizes were found to be few tens of Nano meters and increased with annealing temperature. According to group theory, there are six Raman active modes $A_{1g}+2B_{1g}+3E_g$. Raman spectrum confirms the presence of well-crystallized anatase phase of titanium dioxide film. The CV curve and obtained value 27 of dielectric constant shows that titanium dioxide film may be used as high-κ dielectric material to increase the reliability of thin gate oxide for futuristic MOS devices. Also the obtained values of various parameters from C-V curve support the replacement of conventional SiO_2 layer with TiO_2. The porous nature is evident from the FESEM image and is inherent characteristic of the films deposited by Sol-Gel technique. The interface between the gate dielectric and the substrate is a critical part of the MOS device. The higher values of oxide charge interface trap density and leakage current may be related to porous nature of the oxide film. So the

leakage current values below 100 mA/cm^2 may be acceptable in microelectronics industry for the fabrication of high performance and low power circuits logic circuits. Further improvements in deposition and annealing process are required to make these films suitable for MOS devices. This may results to increase in reliability of thin gate oxide. Considering the low cost TiO_2 thin films grown over SiO_2 could be promising candidate as high-κ dielectric in CMOS devices. More research is needed in case of TiO_2 to solve leakage current problem without decreasing in effective dielectric constant.

CONCLUSION

TiO_2 thin films prepared by sol-gel method on silicon substrate were deposited successfully and found porous in nature. The band gap was calculated 3.6 eV hence the material may be most suitable for solar cells. The capacitor uses Si substrate with aluminum as another terminal. The dielectric constant of TiO_2 film of thickness 52 nm was found 27. Further improvements are necessary in deposition process and annealing process in order to bring the interface trap charge density and leakage current value at minimum level however the MOS capacitance is very high in comparison with SiO_2 MOS capacitor. Anatase TiO_2 thin films prepared by sol-gel method may be considered for the fabrication of various applications as photovoltaic cells and in microelectronics devices.

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