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Research Article
dB-Linear Variable Gain Amplifier Design in 0.18 µm Process with Optimization

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Abstract

Background and Objective: Based on the different gain switching mechanisms, variable gain amplifiers can be categorized as analog controlled VGA and digital controlled programmable gain amplifier (DVGA). A complementary metal oxide semiconductor (CMOS) linear-in-dB variable gain amplifier (VGA) design in TSMC 0.18 µm process was presented and a new approach was proposed in this study. **Materials and Methods:** The proposed circuit is composed of two trans-impedance amplifiers and trans-conductance amplifier. Flexibility was ensured to VGA control using a novel method based on active resistor implemented. VGA control is ensured by using analog voltage control (Vctr). The optimized circuit presents high gain, high bandwidth, low power consumption and low noise figure (NF). The dB-linear gain is controlled linearly by the gate voltage, resulting in a simple and robust VGA. **Results:** Based on the novel technique of degeneration resistor which improves the gain range, a 64.02 dB (23.37-40.65dB) continuous gain range is achieved with a single-stage structure. The simulation structure provides a maximum gain of 40.65 dB over more than 450 MHz bandwidth and less than 16.9 dB of NF. Under 1.8 V supply voltage, the current consumption of the VGA is 40 µA. The input-referred in-band noise density is 5.40 nV^2/Hz and the third order intercept point measured at the input (IIP3) of 4 dBm. **Conclusion:** Simulations results illustrate the best gain range as well as bandwidth performance by tuning the bias gate voltage V_{ctr}. The proposed VGA is one of the best in terms of dynamic range, number of stages and power consumption. Furthermore, it has competitive performance regarding the other parameters.

Key words: Variable gain amplifier, dB-linear, analog control, complementary metal oxide semiconductor, gain range, degeneration resistor, optimization

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Data Availability: All relevant data are within the paper and its supporting information files.

INTRODUCTION

The design of receivers includes different blocks such as filters, low noise amplifiers, gain controlled amplifiers, mixers and analog to digital converters. Automatic gain control (AGC) constitutes one of the most important components in wire and wireless communications where incoming signals with a high dynamic range are treated[1,2]. In this context, variable gain amplifier (VGA) is an indispensable block in the AGC system since it ensures the receiver gain regulation[3]. Nowadays, for the reconfigurable receiver system, the filtered signal is fed into a VGA, which also allows for coarse dc offset correction (DCOC) and provides further low-pass filtering using an additional pole. This stage provides sufficient gain for weak signals to meet the sensitivity requirements and enough attenuation for strong signals to prevent overdriving the ADC[4]. It is one of the critical components in modern wireless communication multistandard receivers[5].

The variable gain amplifier (VGA) is widely used to provide a fixed output power for different input signals to improve the transceiver's dynamic range[1]. It is one of the critical components in modern wireless transceiver designs[1-9]. The location of the VGA in a RF system is circled by dashed line as shown in Fig. 1. The frequency bandwidth is selected using radio frequency (RF) filters. The RF selected signal is then amplified by the large bandwidth low noise amplifier (LNA) or a single multi-band LNA, before being down converted into the base-band using the mixer. The VGA can be placed either before or after channel selection filter, based on actual requirement of amplification first or filtering first.

In wireless communication receiver designs, there is a significant amount of the propagation effects and change of the position or direction of the antenna, due to channel fading. These variations are even more numerous when the receiver moves. Thus, designing such a block becomes a delicate task. So that, the gain variation range should be large enough to cover the whole possible input signal range and it is the best to be dB-linear. Large gain variation range or dB-linear gain range can be realized in a single stage or by cascading multiple stages. Cascading multiple stages usually result in higher power consumption, larger die area and poorer linearity and noise performance.

The aim of this study was to use one stage of VGA instead of cascading two VGA cells as it was presented in Lahiani *et al.*[6] and Ayadi *et al.*[10] with a new structure of degeneration resistor. A novel "cell" structure has been presented to demonstrate the performance enhancement with the use of only one VGA stage for a maximum gain and a minimum area[11,12]. Designing a general purpose VGA to large gain variation range, low power, low noise, wide bandwidth and high linearity is in all likelihood impossible. Several design trade-offs must be taken into account to meet different system specifications.

Based on the different gain switching mechanisms, variable gain amplifiers can be categorized as analog controlled VGA and digital controlled programmable gain amplifier (DVGA). The VGAs are tuned continuously by analog control signals, whereas DVGAs are tuned discretely by digital control signals. Although the design specifications of a VGA/DVGA can vary significantly in terms of bandwidth, power consumption, noise and linearity for different applications, a common specification of the VGA/DVGA is to accurately realize the dB-linear characteristic.

In this study, a new approach was proposed to present single stage VGA for a large gain variation range, maximum gain and a minimum area.

MATERIALS AND METHODS

Circuit design of the proposed VGA cell: The VGA cell was a fully differential pair with source degeneration as presented in Fig. 2. The adopted architecture is detailed in Ayadi *et al.*[10], Thanachayanont[13], Lahiani *et al.*[14,15]. This structure is obtained by cascading and trans-conductance amplifier and a

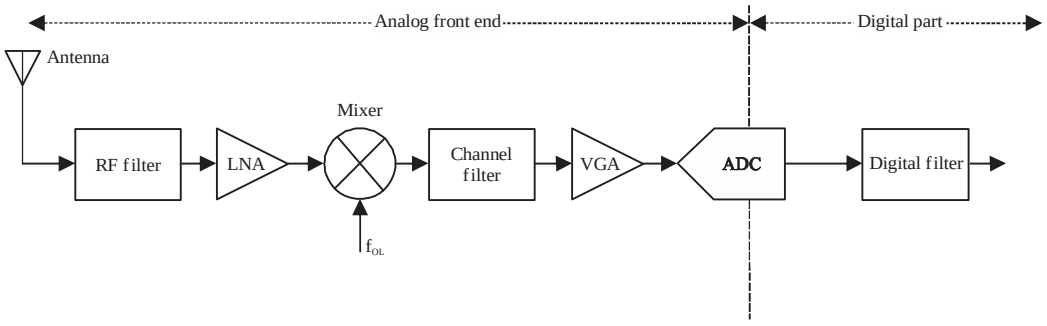

Fig. 1: A simple RF system showing the location of VGA

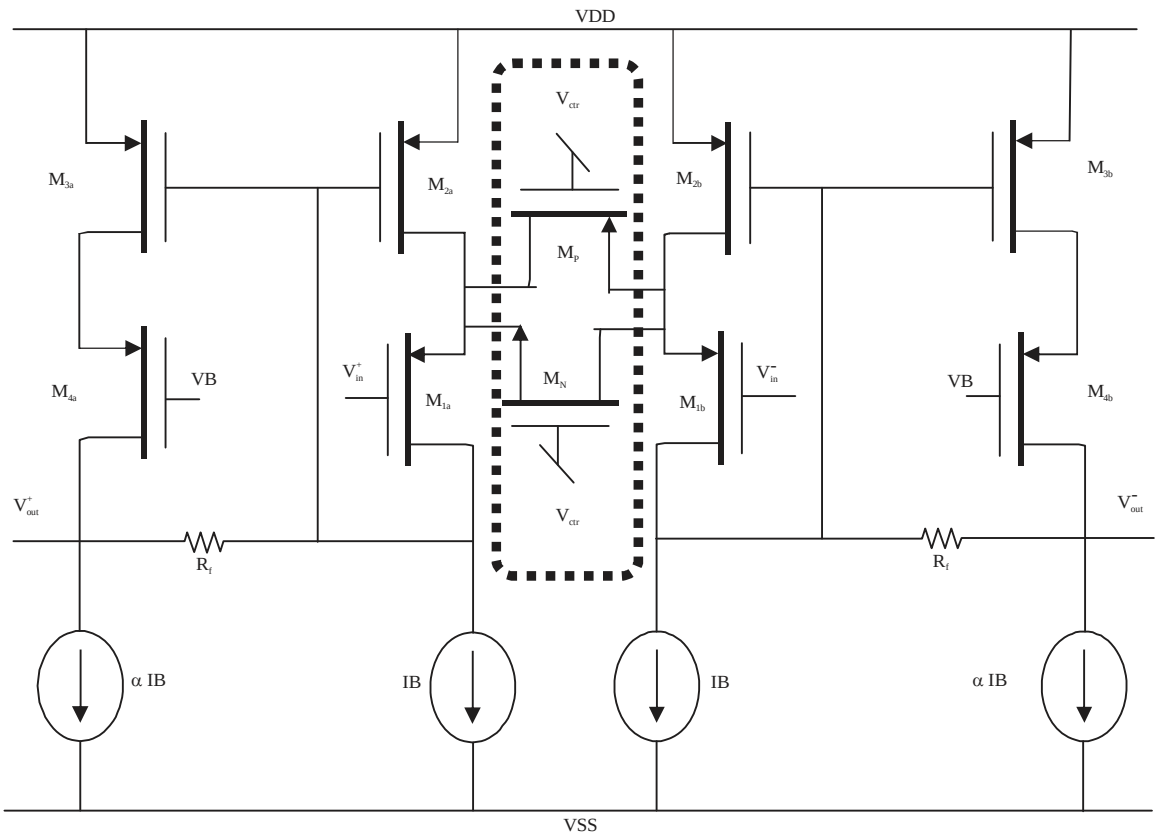

Fig. 2: Analog VGA cell electrical design with novel degeneration resistor architecture

trans-impedance amplifier. The trans-impedance amplifier is performed using a current amplifier with feedback resistors (Rf). The differential pair with variable degenerative resistor, shown in Fig. 2, is a very popular standard topology for a differential variable-gain amplifier since it offers a good trade-off between linearity, gain range and power consumption. The differential input signal is copied over the series impedance of the two nonlinear trans-conductances and the linear degeneration resistor resulting in a differential signal current. In this study, the source degeneration resistor Rs[16] is implemented using a linear function in CMOS that can be realized by biasing the transistor in triode region. The proposed architecture of VGA allows a good gain variation range by the slope of the linear function. Another advantage of this structure is that the bandwidth is largest, which may be available for standard CMOS technology which required a high bandwidth.

The analog VGA cell operation can be explained briefly as follows: A differential input voltage is applied at $M_{1a,1b}$ PMOS transistor. It is reproduced across the source degeneration resistor which is presented by the transistors M_N and M_P, causing the reproduction of current signal into $M_{2a,2b}$.

In this study, the source degeneration resistor is implemented using the transistors M_N and M_P. The implementation of a linear function in CMOS can be realized by biasing the transistor M_N and M_P in triode region, the bandwidth of this structure is good. The gain variation range of the VGA is controlled by the voltage control V_{ctr}. The studied structure is used in current amplification is then ensured by mean of the two trans-impedance amplifiers. The amplified current is converted to an output voltage signal via the feedback resistor RF. The proposed analog VGA is based on simplifies the gain control technique by varying the voltage control V_{ctr}. Current sources are implemented using cascode current mirrors.

VGA requirements and challenges

Gain variation range: The gain variation range should be large enough to cover the whole possible input signal range and is best to be dB-linear. Large gain variation range or dB-linear gain range can be realized in a single stage or by cascading multiple stages. Cascading multiple stages usually result in higher power consumption, larger die area and poorer linearity and noise performance.

The DC voltage gain A_{DC} can be approximated as Eq. 1[10]:

$$A_{DC} = \frac{-\left(\frac{1}{g_{m3}} + R_f\right)\left(\frac{\alpha}{\alpha+1}\right)}{\left(g_{MN,MP} // r_{02}\right)\left(1+\frac{R_f}{(1+\alpha)r_{0c}}\right)} \approx \frac{R_f}{\left(g_{MN,MP} \times \frac{\alpha}{\alpha+1}\right)} \quad (1)$$

Where:

α = A mirror ratio
R_f = The shunt feedback resistor
$g_{MN,MP}$ = The trans-conductance of the transistors M_N and M_P
r_{02} = The drain-source resistance of transistor $M_{2a,b}$
r_{0c} = The current mirror output resistance which is given by Eq. 2[10]:

$$r_{0c} = g_{m4} r_{04} r_{03} \quad (2)$$

where, g_{m4} is the trans-conductance of the transistors M_4, r_{04} and r_{03} are respectively the drain-source resistance of transistor M_4 and M_3.

Bandwidth: The VGAs can be categorized into two types based on the targeted operation frequency range. One type is general purpose VGA, whose bandwidth is normally much larger than required, for low bandwidth applications. The other type is high-frequency VGA, whose bandwidth is very large as they are designed for advanced communication scheme where bandwidth requirement is very stringent.

Noise and linearity: The noise and linearity performance of a VGA are crucial. Noise is mostly related to the sensitivity of the VGA, which determines the smallest signal that a VGA can amplify. Linearity is mostly related to the compression or saturation due to circuit nonlinearity, which in contrast determines the largest signal that a VGA can amplify. Obviously that low noise and high linearity are desirable.

Considering only thermal noise sources, the VGA cell input-referred mean-square noise can be approximately calculated as given by Eq. 3[10]:

$$\overline{v_{ni}^2} \approx -\frac{1}{g_{m1}^2}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2}\right) + \frac{1}{g_{MN,MP}^2}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2}\right) + \overline{v_{n,Rf}^2}\left|\frac{1}{A_{DC}}\right|^2 + \overline{i_{n3}^2}\left|\frac{1+g_{m1}g_{MN,MP}\left(1+g_{m2}R_f\right)}{g_{m1}\left(-1+g_{m3}R_f\right)}\right| \quad (3)$$

where, $\overline{v_{n3}^2}$ and $\overline{v_{n,Rf}^2}$ are respectively the input referred thermal noise voltage of the transconductance amplifier, the input referred thermal noise voltage of R_f. $g_{MN,MP}$ and g_{m1} are respectively the trans-conductance of the transistors M_N, M_P and M_1 transistors. A_{DC} is the DC voltage gain.

Power and supply voltage: The power consumption of a VGA is crucial especially for low power applications. The power consumption has to be small to extend the battery life as well as to generate less heat. The challenge of ultra-low power VGA design is mainly the noise and linearity degradation, which then significantly deteriorates the overall performance of the VGA.

Analog VGA cell optimization

Problem formulation: The Heuristic algorithm used for optimizing the proposed VGA performances is essentially a random process, it consists on the following steps:

- The building of mathematical models for both constraints and preliminary conditions to satisfy. This program gives all possible quiescent parameters which are candidate for the optimization
- Performance criteria and error sources are mathematically modelled. These models are then taken into consideration in the program and optimal parameters can be randomly selected between the already calculated quiescent parameters
- The optimization approach follows the plot depicted in Fig. 3. In fact, the Heuristic is an algorithm driven methodology which consists on maximizing gain value, maximizing bandwidth values and minimizing noise effect and silicon area. Taking into consideration these performances and error functions, the objective function F (expression 4) is a weighted sum of these criteria. Since these functions have different quantity types with different range of variations

Optimization approach: In order to optimally size each component forming the analog VGA cell when satisfying constraints and performance functions, we developed an algorithm that allows automating the task[17-19]. This algorithm was programmed using C^{++} software. It is based on the flow chart given by Fig. 3. It describes an optimization tool based on Heuristic algorithms.

The first step in the optimization is the expression of the different criteria by a technology dependent model. For accurate modeling, a small signal analysis of the VGA is carried out to explicit the different characteristics intended optimized. The following series of criteria was used in VGA optimization[20]:

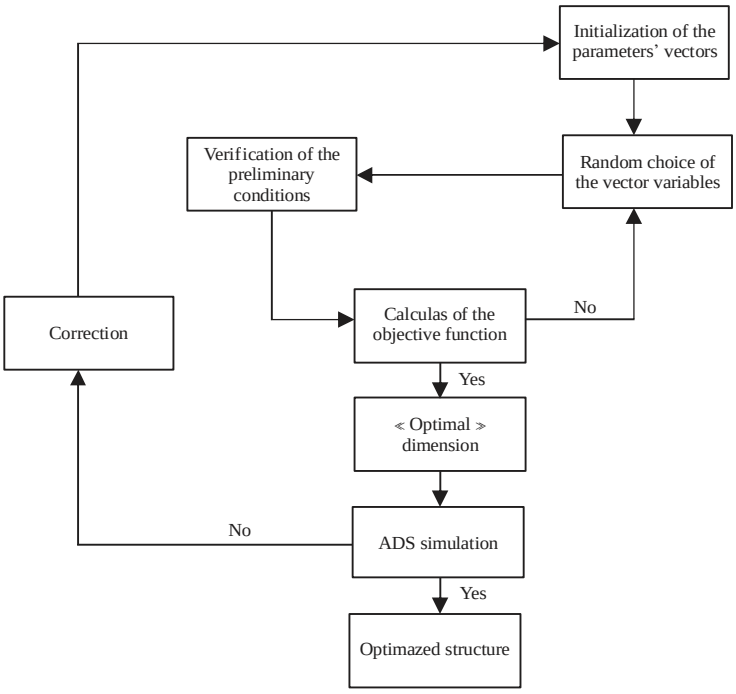

Fig. 3: Optimization algorithm flow chart

- The gain Av is maximized
- The dominant frequency is maximized
- The input referred noise (VT,in) is minimized
- The silicon area is minimized

The objective function "F" to maximize can thus be formulated by Eq. 4[14]:

$$F = a_1 A_v + a_2 f_{-3dB} + \frac{a_3}{v_{in,th}^2} + \frac{a_4}{NF} + \frac{a_5}{W_i L_i} \quad (4)$$

After several iterations, many valid vectors test were obtained. The transistors sizing of the VGA circuit are planned in Table 1.

The proposed VGA cell is simulated using the advanced design system (ADS) tool with TSMC 0.18 µm CMOS process parameters under 1.8 V power supply. The NMOS and the PMOS transistor threshold voltages are respectively 0.436 and -0.438 V[9]. The optimized value of bias current is set to 40 µA. Current sources are implemented using cascode current mirrors.

Table 1: Transistors sizing

Transistors	W (µm)	L (µm)
M_{1a}-M_{1b}	10	0.18
M_{2a}-M_{2b}	5	0.18
M_{3a}-M_{3b}	15	0.18
M_{4a}-M_{4b}	30	0.18
MN-MP	50	

RESULTS AND DISCUSSION

VGA circuit simulations: The gain variation of this analog VGA cell topology is allowed by varying the analog voltage control V_{ctr}. Accordingly, simulations are accomplished in order to follow up gain and noise figure fluctuation when V_{ctr} tuned from -0.5 V to 0.5 V. Figure 4 presents the variations versus the V_{ctr}.

Figure 5 shows the simulated dB-linear gain characteristics of the proposed gate-tuned VGA. The dB-linear range is achieved to 73.02 dB.

The high gain is obtained by maximizing V_{ctr} to 0.5 V. Figure 6 depicts that the maximum gain obtained by one VGA cell is above 40.65 dB. The corresponding NF curve is shown in Fig. 7. The Noise is equal to 16.98 dB.

Figure 8 depicts the input referred noise (IRN) value of the proposed VGA over the 10-500 MHz frequency band and for several gain settings. The VGA input referred noise is around 5.403 nV^2/Hz.

By adjusting V_{ctr} to -0.5 V, Fig. 9 is obtained showing the minimum gain of one VGA cell which is around -23.37 dB. The corresponding noise which its value is 18.54 dB is illustrated in Fig. 10.

Figure 11 shows the IIP3 simulation curve. The IIP3 is equal to 4 dBm at the gain condition of 40.65 dB.

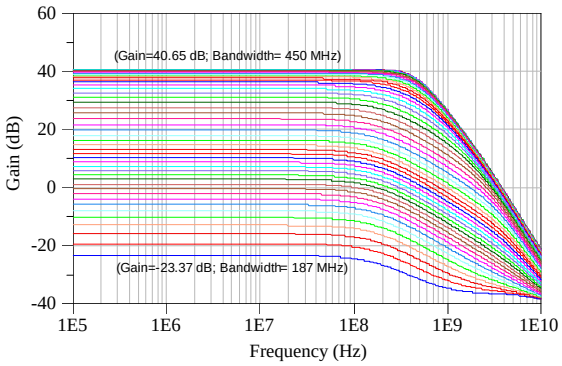

Fig. 4: VGA gain for different analog control voltage V_{ctr}

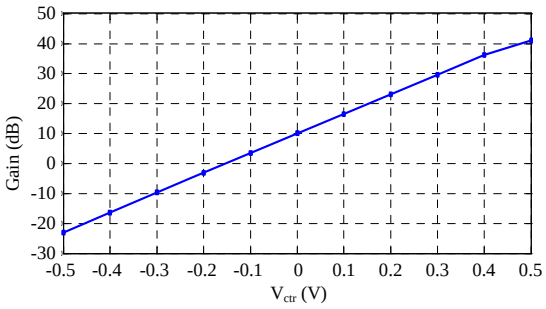

Fig. 5: Gain of the proposed VGA

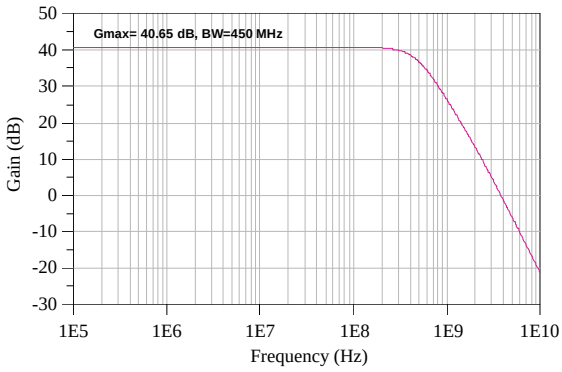

Fig. 6: Maximum voltage gain response

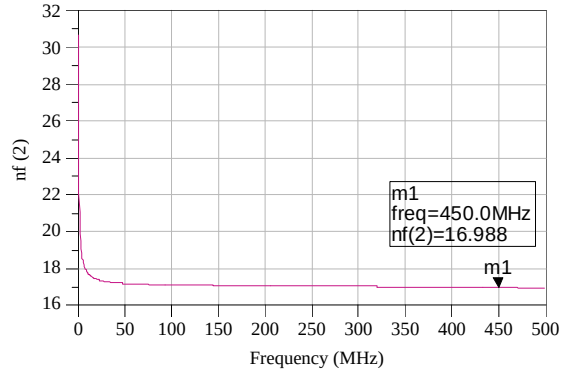

Fig. 7: Noise figure curve

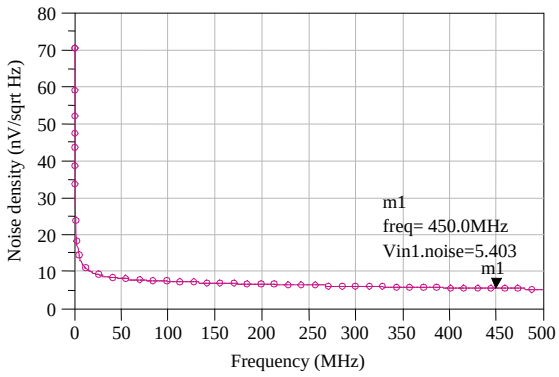

Fig. 8: Input-referred noise curve

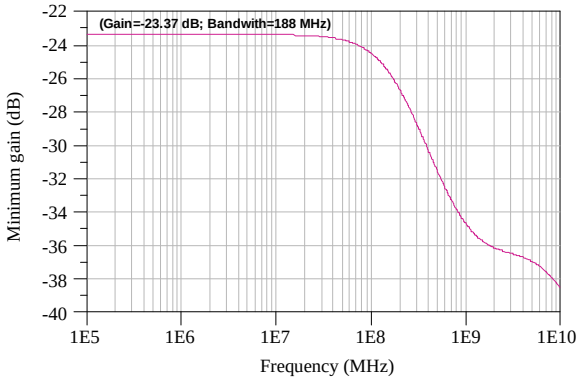

Fig. 9: Minimum voltage gain

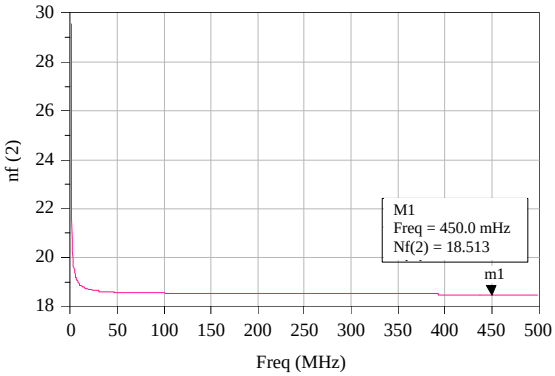

Fig. 10: Noise figure response for minimum gain

A simple cell-based approach is presented for the design of low power and high frequency VGA. To utilize the proposed approach, the design and analysis of a unique gate tuned VGA cell has been presented, which utilizes complementary transistors for realizing a linear function. Since this gate-tuned VGA cell requires no extra circuit to generate an exponential-like function, it drastically reduces the power consumption. Therefore, the presented approach is suitable for many applications, where low power, high frequency and accurate dB-linear characteristic are required.

Table 2: Comparison with recent study

Parameters	Hur and Eisenstadt[21]	Wang *et al.*[22]	Choi *et al.*[16]	Onet *et al.*[12]	Ayadi *et al.*[10]	Liu *et al.*[23]	Wang and Zhu[24]	Proposed structure
Gain range (dB)	0~2.5	-10~50	-13 ~ 63	-5.5~28	20.3~74.02	3.6 ~59.6	-35~ 28	-23.3~40.6
dB linear range (dB)	2.5	60	50	-	-	56	-	64.02
Bandwidth (MHz)	80~9000	2200	14.8	0.7 ~60	10.40	63.5	47~640	450
NF (dB)	9.5	17~30	-	27.1	19.38	-	-	16.9
IRN (nV^2/Hz)	-	-	3.5	11.4	-	10.6	-	5.40
Number of Stages	4	4	3	1	3	15	1	1
IIP3 (dBm)	12.5	-13 to 55	11.5	-11.8 to 18.3	-5.5	8	8	4
Supply Voltage (V)	3.1	1	1.2	1.8	1.5	1.8	1.8	1.8
Power consumption (µW)	40m	2.5m	0.6	7.54	15m	1.12	3.5	82
CMOS Process (µm)	0.13	90	65	0.15	0.35	0.18	0.18	0.18

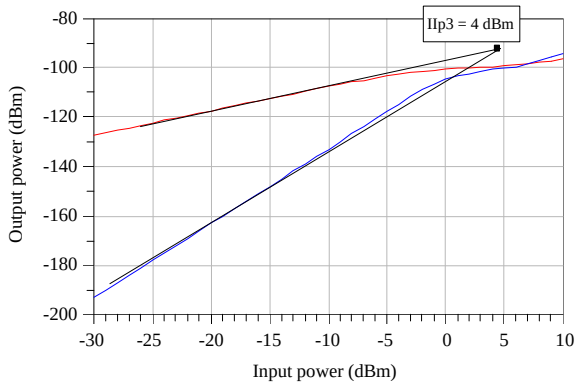

Fig. 11: IIP3 simulation curve

A comparative study of VGA cell between this study and recent researches is depicted in Table 2. From the Table, it is evident that the circuit is able to vary the voltage gain in linear dB from -23.37 to 40.65 dB. The total power consumption is less than 82 µW from a 1.8 V power supply having a wide and constant bandwidth, which is better than reported in Ayadi *et al.*[10] and Liu *et al.*[23]. In comparison with recent researches, the proposed VGA is one of the best in terms of dynamic range, bandwidth, number of stages and power consumption. Furthermore, it has competitive performance regarding the other parameters. It is, therefore, clear that the proposed VGA can be used in wide band applications such as Ultra Wide Band (UWB) standard.

CONCLUSION

In this study, a novel linear approximation method for a dB-linear VGA is presented. The proposed approximation does not require an extra circuit for generating the linear function and it drastically reduces design complexity and chip area. Moreover, the dB-linear gain can be controlled easily using the voltage gate bias.

SIGNIFICANCE STATEMENT

The study presents a new compact single-stage variable gain amplifier (VGA) architecture design. In this study designed one stage of VGA instead of cascading two VGA cells with a new structure of degeneration resistor which is used for low power applications. In addition, the optimized VGA circuit has competitive performances regarding the gain range, the bandwidth, the noise figure and the power consumption. It is clearly seen that reach a low power topology with a high dynamic range.

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