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Low Voltage High Frequency CCII Based Multifunction Filters and Chaos Generator

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ABSTRACT

This study deals with optimization of a high frequency Current Conveyor (CCII) at low supply voltage. The optimized structure is then applied in the design of a high frequency multifunction tunable filter and a chaos generator. Firstly, heuristic algorithm is used for optimal sizing regarding static and dynamic performances. An optimal sizing of a low voltage low power CMOS Current Conveyor (CCII) was then done. The optimized CCII configuration has a current bandwidth of 1.53 GHz and a voltage bandwidth of 1.406 GHz and 190 Ω as Rx parasitic resistance value. Secondly, implementation of an ameliorated multifunction filter based on this configuration was presented and a new RLC low voltage chaos generator using the second-generation current conveyor (CCII) as active building block is presented. The current mode filter has a tunable central frequency in the range [480-638 MHz]. PSPICE simulations are presented to demonstrate these results.

Key words: Low voltage, second generation current conveyor, multifunction filters, current conveyor, optimizing heuristic

INTRODUCTION

In 1970, the second generation was proposed for various applications such as amplifiers (Fabre *et al*., 1996; Erdal *et al*., 2001), filters (Salem *et al*., 2006; Garcia-Ortega *et al*., 2007; Masmoudi *et al*., 2005), oscillators and chaos generator (Masmoudi and Fakhfakh, 2004; Elwakil and Soliman, 1999) or more generally signal processing circuits. Owing to their extra modularity, current controlled design features was achieved. Such control is of great importance, namely in telecommunication applications. The use of low voltage to get low power is well established in analogue circuits for the telecommunication application. A lot of varieties of CCII electronic implementations were proposed, having as motivation power supply reduction and high frequency operations. However, the proposed CMOS CCII based applications do not resolve the high frequency limitations. Recently, in CMOS process, current mode circuits have seen a tremendous increasing of the frequency response (Ahmed and Soliman, 2011). Extrapolating these performances to CCII based circuits is still open (Sedra and Smith, 1970). A considerable amount of signals in analog and digital signal processing is usually required.

The CCII is a three terminal active block. Its general representation is shown in Fig. 1. The CCII ensures two functionalities between its terminals:

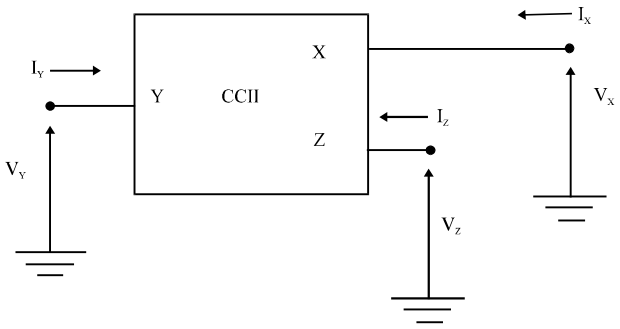

Fig. 1: General representation of current conveyor

- A current follower between terminals X and Z
- A voltage follower between terminals X and Y

In order to get ideal transfers, a CCII should be characterized by low impedance on terminal X and high impedance on terminal Y and Z.

Taking into account parasitic impedances, the CCII behavior can be described in the following relation:

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} \dfrac{1}{R_Y // C_Y} & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \alpha & \dfrac{1}{R_Z // C_Z} \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \quad (1)$$

where, α and β are current and voltage transfers of the CCII. RY , CY and RZ, CZ are parasitic resistances on port Y and Z, respectively, they are ideally infinite impedances. RX is the parasitic resistance at port X being ideally a short circuit.

In this study, a new configuration is proposed to realize current mode multifunction filter and chaos generator simultaneously by using:

- Two optimized low supply voltage of CCII and two CMOS Varactors for the filter
- An active inductor, non-linear resistor, two grounded capacitors and one resistor for the chaos generator

LOW VOLTAGE CCII CONFIGURATION

Several current conveyor structures have been proposed in the study. Looking at high frequencies operations, we optimize performances of this structure, thanks to the heuristic that we develop in the next section. Being attracted by low voltage operations, we consider the CCII configuration depicted in Fig. 2 (Masmoudi and Fakhfakh, 2004).

Over the years, several current conveyor structures have been proposed. The second-generation configuration is the most well known one owing to its performances. Let's consider the CCII configuration in Fig. 2 in a 0.35 μm MOS technology. Assuming the same gain factors for the

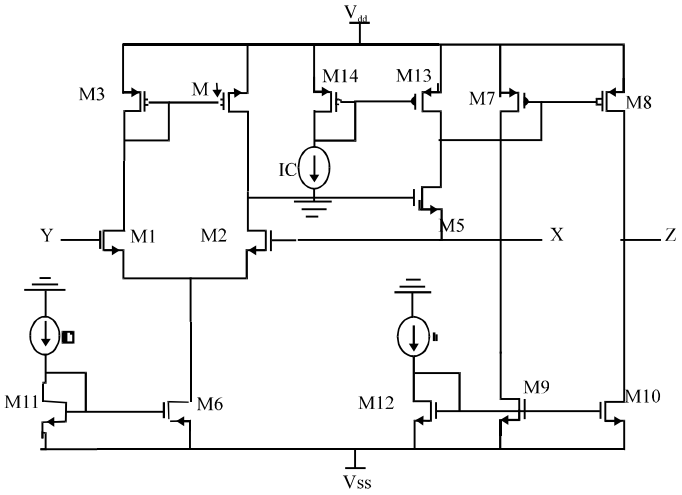

Fig. 2: Low supply voltage CCII

NMOS and PMOS transistors, the parasitic impedances, the current bandwidth and the voltage bandwidth are given by the following Equations:

$$Rx = \frac{rds_{13}rds_5}{1 + \frac{(rds_{13}rds_5)(rds_7 + rds_8)}{(rds_7rds_8)}} \tag{2}$$

$$Rz = \frac{rds_8rds_{10}}{rds_8 + rds_{10}} \tag{3}$$

$$f_{ci} = \frac{a_0 + a_1p + a_2p^2 + a_3p^3 + a_4p^4}{b_0 + b_1p + b_2p^2 + b_3p^3 + b_4p^4 + b_5p^5} \tag{4}$$

$$f_{cv} = \frac{e_0 + e_1p + e_2p^2 + e_3p^3}{q_0 + q_1p + q_2p^2 + q_3p^3} \tag{5}$$

where, a0,..., a4, b0,...., b5, q0,..., q3 and e0,...., e3 are coefficients that depend on technology parameters and transistors sizing.

THE OPTIMIZATION HEURISTIC

The heuristic (Bensalem *et al.*, 2004; Fakhfakh *et al.*, 2004; Ben Said *et al.*, 2007) used to optimizing current conveyor performances is essentially a random procedure; it consists of the following steps: "The first step consists of building mathematical models for both constraints and preliminary conditions to satisfy. All relations were programmed by means of C++ software. This program gives all possible quiescent parameters which are candidate for the second optimization step". The second step is the optimization approach. Firstly, performance and error sources are

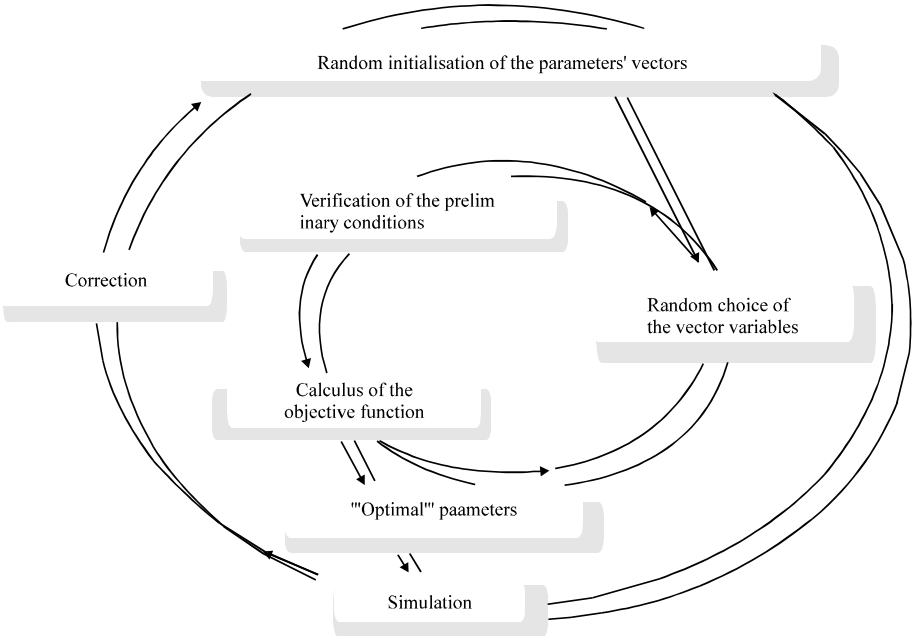

Fig. 3: The heuristic approach

mathematically modeled. These relations are then taken into consideration in the C++ program thus optimal parameters can be randomly selected between the already calculated quiescent parameters. Then a function of merit Fob was considered for this purpose; it is given by Eq. 6:

$$Fob = \frac{a_1}{Fci} + \frac{a2}{Fcv} + \frac{a_3}{Rz} + a4 \times Rx \tag{6}$$

where, $\alpha 1,..., \alpha 4$ are positive coefficients used for normalization, Fci and Fcv are the cut-off frequencies of the current follower and the voltage follower, respectively. It is important to notice that for a precise convergence of the algorithm to optimal parameters, we need to correct constants values such as those used for the calculus of MOS conductance. So we have to do simulations with the obtained parameters then correct constants values and re-run the algorithm and so on until full convergence of obtained results. Figure 3 summarizes different steps of this optimization procedure.

In fact, the Heuristic is an algorithm driven methodology which consists of minimizing X port input resistance value, maximizing Z port resistance value, maximizing high cutoff current and voltage frequencies. Taking to consideration these performances the objective function Fob is built. In this application, we need to maximize the objective function given in Eq. 6. Simulation conditions are summarized in Table 1.

Owing to the heuristic detailed above optimal sizing of each transistor in the current conveyor are obtained in Table 2.

The optimized current conveyor was simulated with SPICE software. Main obtained results are represented in Fig. 4-9.

Figure 4 and 5 show hat the low values of Rx can be controlled between 18 and 275 Ω while Ic covers the range [1-200 μA] and R_Z can be controlled between 18 and 45 kΩ while Ib covers the range [1-200 μA].

Table 1: Simulation conditions

Technology	0.35 µm CMOS AMS
Supply voltage	-1.05/1.95 V
Bias current (Ib)	200 µA
Bias current (Ic)	10 µA
Bias current (Io)	50 µA

Table 2: Optimal device sizing

Device name	Aspect ratio W/L (µm)
M1, M2	6.5/0.35
M3, M4	19.5/0.35
M5, M6, M9, M10, M11, M12	13/0.35
M7, M8	39/0.35

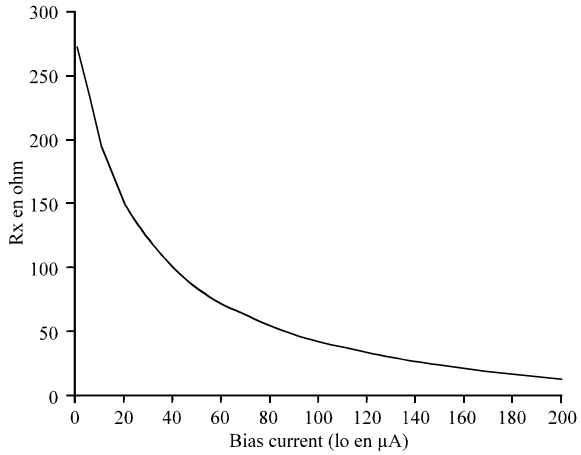

Fig. 4: Parasitic resistance Rx versus the control current Ic

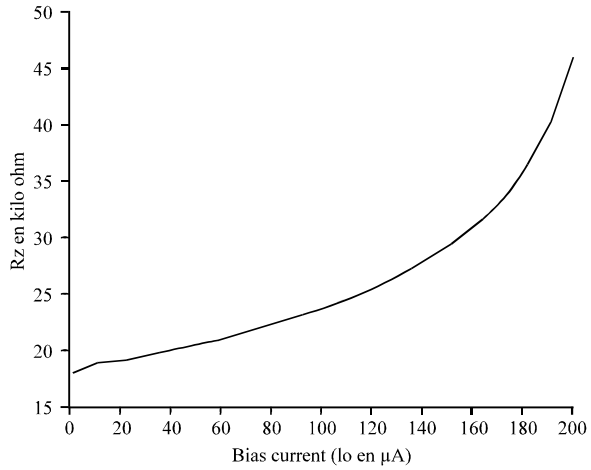

Fig. 5: Parasitic resistance and Rz versus control current Ib

Figure 6 represents non linear dependency between X and Y terminal voltages when input voltage exceeds 75% of power supply voltage. In addition, Fig. 7 illustrates obtained high voltage bandwidth which is equal to 1.53 GHz with a static gain $\beta = 0.96$.

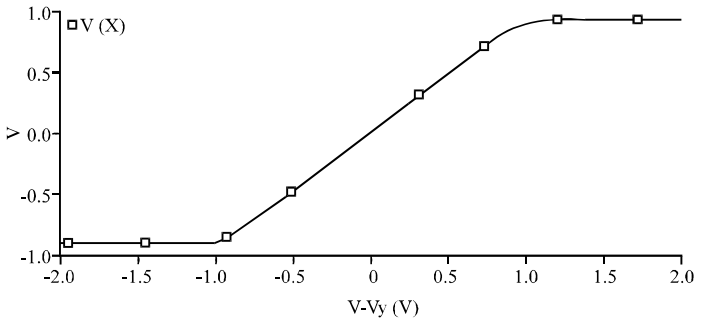

Fig. 6: Voltage transfer between Y and X

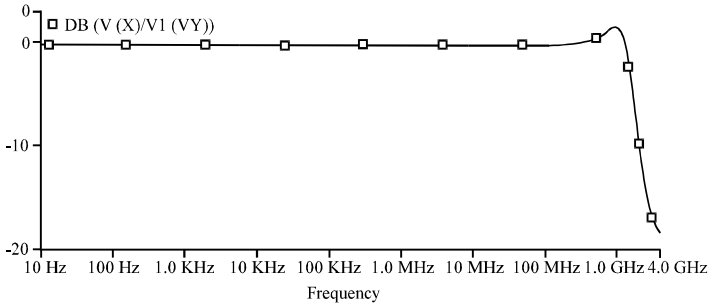

Fig. 7: Gain transfer function between Y and X terminals

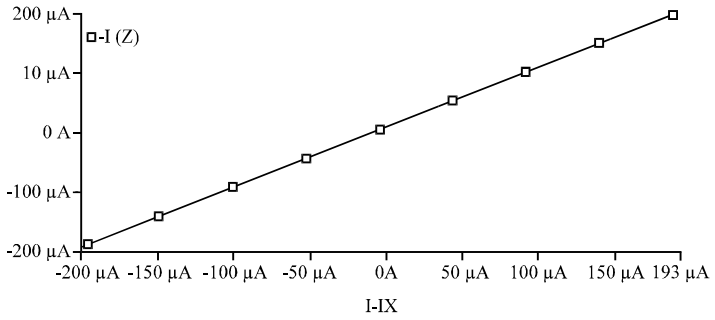

Fig. 8: Current transfer between X and Z

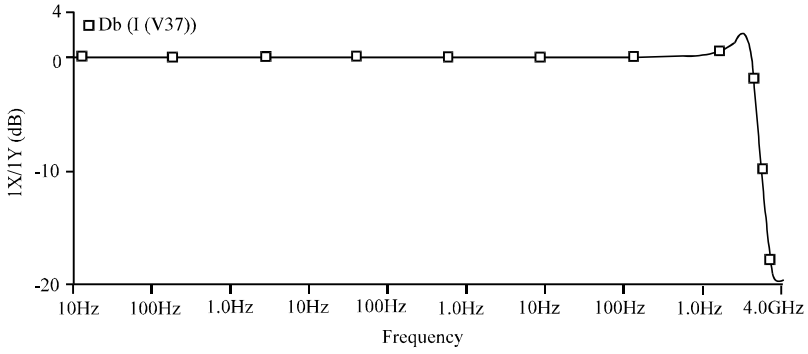

Fig. 9: Gain transfer function between X and Z terminals

On the other hand, current transfer function between X and Z terminals presents an excellent linearity when conveying current. This is illustrated at Fig. 8. Also it is important to put the stress

Table 3: The characteristics of the optimized CCII (with I_b = 200 μA)

Parameters	Obtained results
voltage gain between Y and X ports β(v)	0.961
Current gain between Z and X ports β(i)	1
Current Bandwidth	1.406 GHz
Voltage Bandwidth	1.53 GHz
Offset voltage (Vxoff)	10 mV
Offset current (Izoff)	9 μA
Relative voltage Error(%)	3.44%
Relative current Error(%)t	4.7%
Output impedance (Rz)	20K Ω
Input resistance Rx	190 Ω

on the fact that obtained current bandwidth is equal to 1.4 GHz with a current static gain α equal to 1 as we can see at Fig. 9.

These improved results are summarized in Table 3 where as simulation conditions are given in Table 2.

MULTIFUNCTION FILTER

In Fig. 10, we present a current mode multifunction filter with single current input and three current outputs performing three transfer functions (Sagbas and Fidanboylu, 2004). The filter uses two negative-type second-generation CCII's and two passive elements (capacitors).

Taking into account the parasitic impedances of the CCII's, the transfer function of the different output currents can be formulated as follows:

$$H_1(s) = \frac{I_{out1}}{I_{in}} = \frac{A}{s^2 + s\frac{w_0}{Q} + {w_0}^2} \tag{7}$$

$$H_2(s) = \frac{I_{out2}}{I_{in}} = \frac{s^2}{s^2 + s\frac{w_0}{Q} + {w_0}^2} \tag{8}$$

$$H_3(s) = \frac{I_{out3}}{I_{in}} = \frac{Bs}{s^2 + s\frac{w_0}{Q} + {w_0}^2} \tag{9}$$

where,

$$A = \frac{1}{R_{x1}R_{x2}C_1C_2} \tag{10}$$

$$B = \frac{1}{R_{x1}C_1} \tag{11}$$

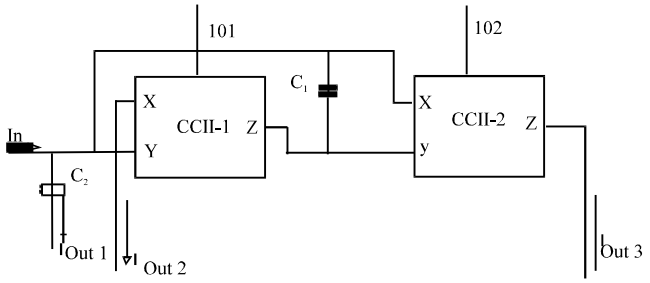

Fig. 10: Current mode multifunction filter

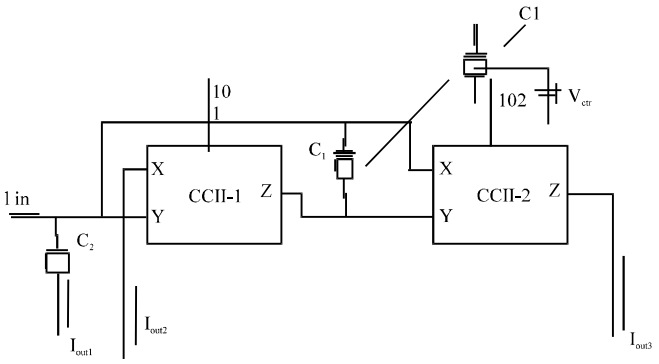

Fig. 11: The proposed current mode multifunction filter

$$w_0 = \frac{1}{\sqrt{R_{x1}R_{x2}C_1C_2}} \tag{12}$$

$$Q = \sqrt{\frac{R_{x1}C_2}{R_{x2}C_1}} \tag{13}$$

Equations 7, 8 and 9 show that the filter can be a Low Pass, a High Pass or a Band Pass one.

In this circuit the center frequency can be adjusted independently of the Q-factor with C1*C2 if the ratio C1/C2 is left constant. It's desirable to adjust the center frequency after integration. For this reason it is not allowed to change the capacitor's values. The first solution is to vary the values of the Rχ1 and Rχ2 (IC1 or IC2). We put the stress on the fact that the natural frequency can be adjusted independently of the Q-factor by action on the product (Rχ1*Rχ2), if the ratio Rχ1/Rχ2 is kept constant. This control can be ensured by varying both currents IC1 and IC2. The second solution is showing in Fig. 11.

In Fig 11 we present the proposed ameliorate multifunction Filter. When we change the capacitor by a CMOS Varactors and we take Vctr1= Vctr2=Vctr (this condition is used to respect the condition: we change C1*C2 and we make invariant the ratio C1/C2).

An implementation of the filter in Fig. 10 was simulated by taking device scaling given in Table 2 and C1 = C2 = 1pF. We thus obtained the central frequency equal to 638 MHz. Figure 12 illustrates the frequency response of the filter.

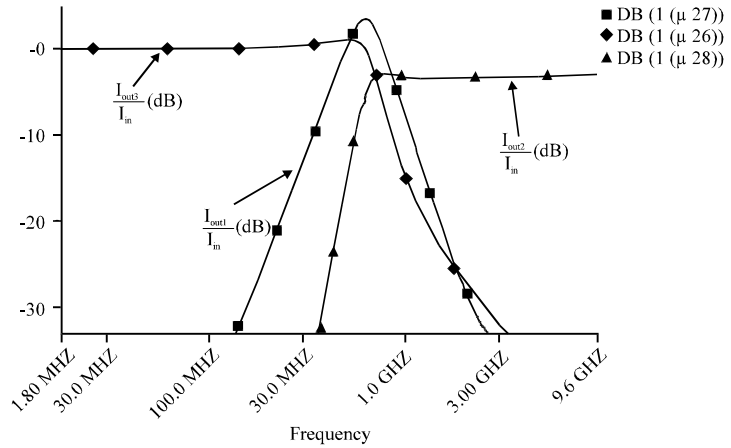

Fig. 12: Simulated outputs of the current mode multifunction filter (I_b = 200 μA and I_C = 10 μA)

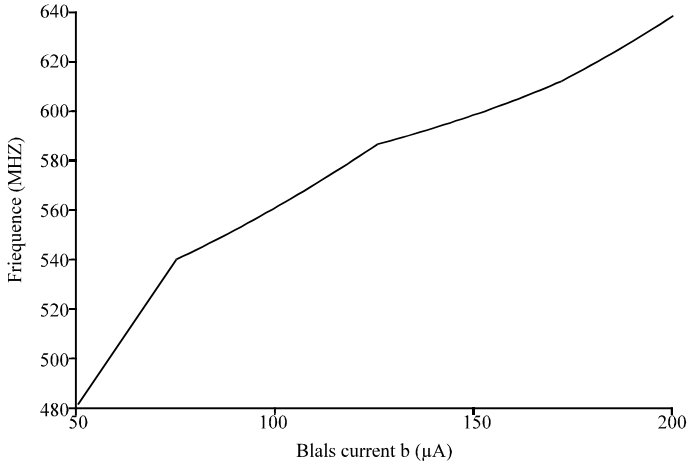

Fig. 13: Central frequency of the filter versus the bias current IC

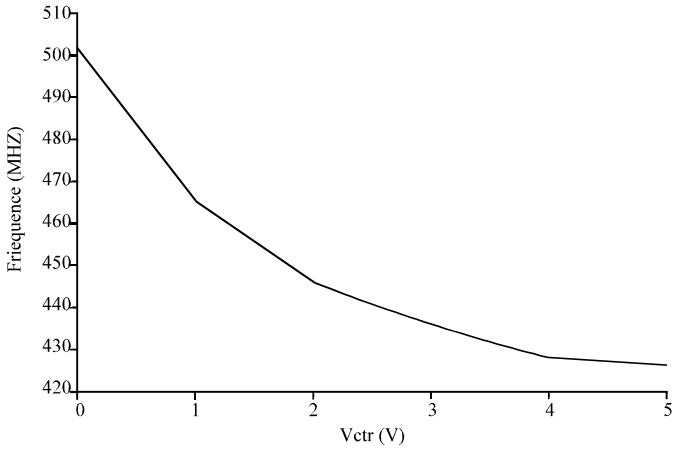

Fig. 14: Central frequency of the filter versus Vctr

An implementation of the filter of Fig.10 was simulated by tuning IC1 and IC2 (IC1=IC2=IC). Figure 13 shows as can be seen the natural frequency can be tuned in the range [480-640MHz].

Moreover the proposed filter is simulated using Pspice for different value of Vctr . Simulation results are shown in Fig.14. We note that by varying the value of voltage (Vctr) between 0V and 5 V, the central frequency is tuned in the range [428MHz- 502MHz].

CCII CHAOS GENERATOR

Chaotic oscillators that are suitable for VLSI integration are advantageous (Kaplan and Glass, 1995; Ben Said *et al*., 2007). The origin of the word chaos is a Greek verb which means to gape open and which was often used to refer to the primeral emptiness of the universe before things came into being. Such systems are defined to be a periodic, bounded dynamics in deterministic systems with sensitive dependence on initial conditions (Feki, 1997). Recently, chaotic signals have shown to be very useful in applications such as signal encryption and secure communication. A simple circuit which is known to exhibit chaos behavior is depicted in Fig. 15, it is referred as Chua circuit (Elwakil and Soliman, 1999; Elabbasy and El-Dessoky, 2007). The Chua's circuit consists of two capacitors C1 and C2, inductor L, a linear resistor R and only one non linear resistor NLR.

The characteristics of the non linear resistor are defined by the curve shown in Fig. 16.

In to three regions in each of which the dynamics is linear so that trajectory can be expressed as a composition of linear flow. Using Kirchoff 's voltage and current laws, this circuit is made by three ordinary differential equations. By choosing Vc1, Vc2 and iL was state variables, we obtain following Equations:

$$\frac{dV_{c1}}{dt} = \frac{1}{RC_1}(V_{c2} - V_{c1}) - \frac{1}{C_1} f(V_{c1}) \tag{14}$$

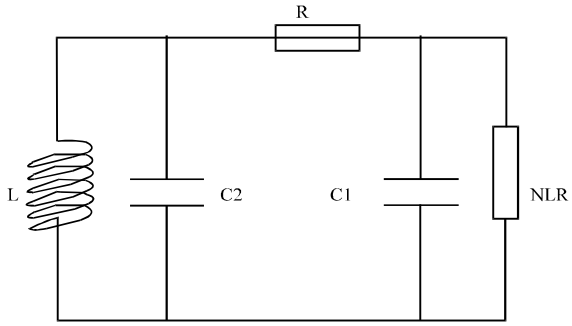

Fig. 15: Chaos Generator

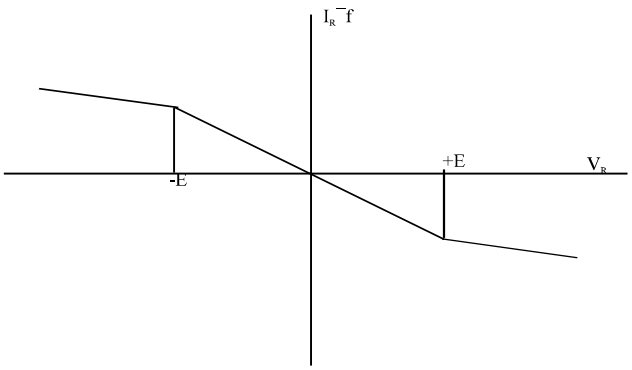

Fig. 16: Nonlinear resistor characteristic

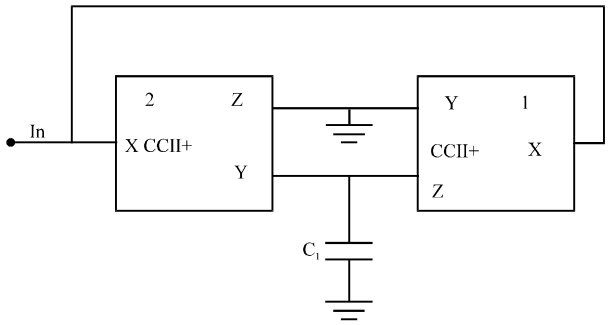

Fig. 17: Implementation of the CCII based inductor

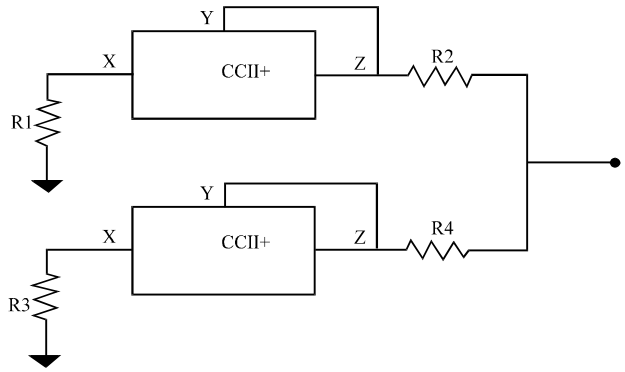

Fig. 18: Implementation of a non-linear resistor using two CCII's

$$\frac{dV_{c2}}{dt} = \frac{1}{RC_2}(V_{c2} - V_{c2}) + \frac{1}{C_2} i_L \tag{15}$$

$$\frac{diL}{dt} = \frac{-1}{L} V_{c2} \tag{16}$$

The Chua's circuit has been implemented in many different ways using standard electronic components and also simple chip integrated circuit. In the modified chaos circuit of Fig. 16, the simple inductor L has been replaced by an active inductor implemented by two CCII and one capacitor (C1 = 10 pF) (Fig. 17, 18):

$$Z_{eq} = R_{x1} // R_{x2} // (jlw) \tag{17}$$

where,

$$L = R_{x1} R_{x2} C_1 \tag{18}$$

The main concern to realize the Chua's circuit is to design the non-linear resistor with the characteristic delineated. Noting that the resistor described there in is active then active device such

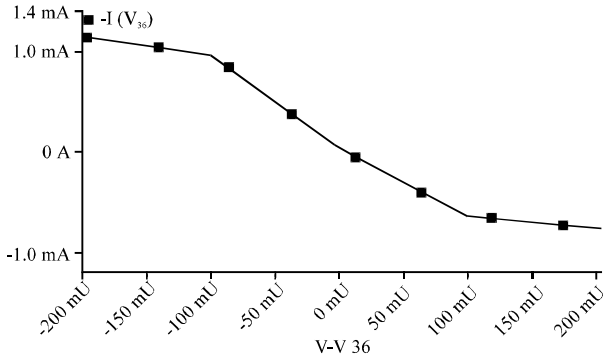

Fig. 19: Nonlinear resistor characteristic

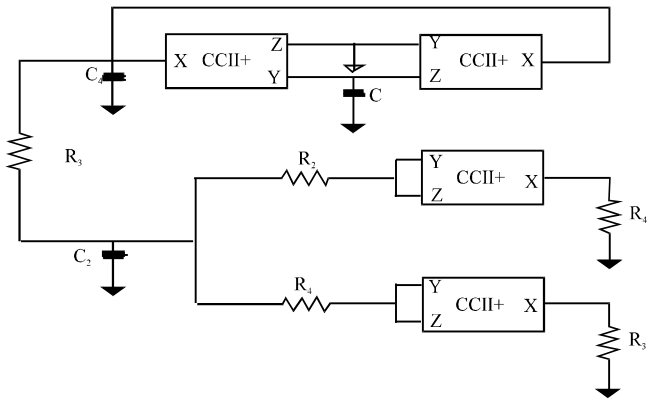

Fig. 20: CCII based chaos generator implementation

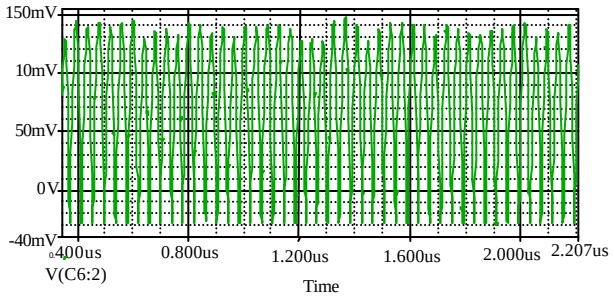

Fig. 21: Time evolution of the state variables VC1

as the CCII should be used. The non-linear resistor is replaced with two CCII optimized and four resistor (R2 = R4 = 10 Ω;R1 = R3 = 100 Ω) (Barthelemy *et al.*, 2002):

$$R_{eq} = \frac{(R_2 - R_{x1} - R_1)(R_4 - R_{x2} - R_3)}{(R_2 - R_{x1} - R_1) + (R_4 - R_{x2} - R_3)} \quad (19)$$

Figure 19 present the characteristic of the non linear resistor. Finally, to implement a complete chaos generator circuit, the simulated inductor has been connected to three passive elements

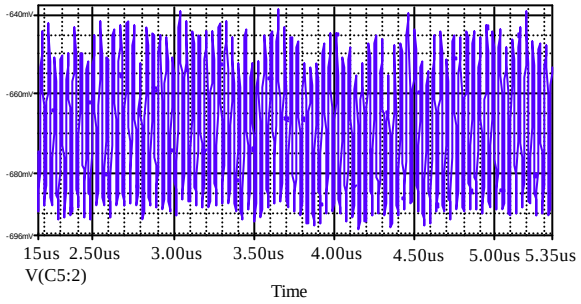

Fig. 22: Time evolution of the state variables VC2

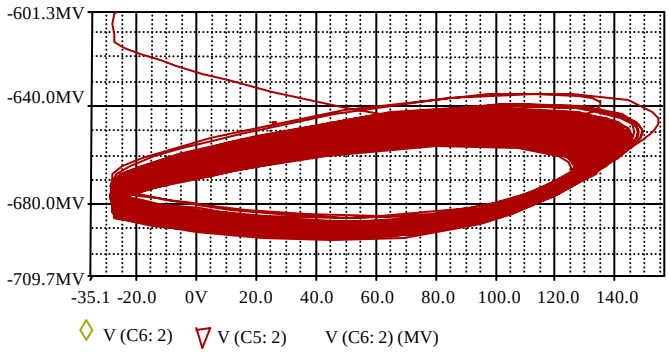

Fig. 23: P-Spice simulation of the chaos circuit ($V_{C2}V_{C1}$ phase portraits)

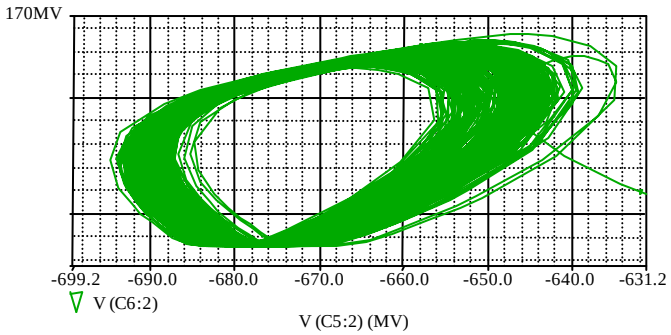

Fig. 24: P-Spice simulation of the chaos circuit ($V_{C1}V_{C2}$ phase portraits)

(2 capacitor (C_1 and C_2) and R_5) and to a non-linear resistor. Figure 20 illustrate the CCII based chaos generator implementation.

The transient responses of the chaotic output voltages V_{C1} and V_{C2} shown in Fig. 21 and 22, respectively illustrate the random magnitude of voltages V_{C1} and V_{C2}. The chaotic nature of the voltages V_{C1} and V_{C2} is further strengthened by the phase plot of Fig. 23 (illustrate the $V_{C2}V_{C1}$ phase portraits) and 24 (illustrate the $V_{C1}V_{C2}$ phase portraits) as the chaotic phase plot displays a complex pattern.

CONCLUSION

In this study high frequency CCII based multifunction filters are presented. An optimized methodology of the Low supply voltage CCII is presented. Simulations of such performances PSpice

software illustrates the very good performances, high cut-off current and voltage frequencies are obtained (the current and voltage bandwidths are respectively 1.53 and 1.406 GHz and the parasitic resistance at port X (Rx) has a value of 190 Ω for a control current of 200 μA). Moreover, we use the optimized improved CCII to build improved CCII based current mode multifunction filters. A current mode filter with a tunable central frequency in the range [480-638MHz] is synthesized.

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