ISSN 1996-3343

Asian Journal of Applied Sciences

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Asian Journal of Applied Sciences 4 (8): 741-751, 2011
ISSN 1996-3343 / DOI: 10.3923/ajaps.2011.741.751

Study of a Mos Condenser with one of his Plates of Fractional Dimension

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ABSTRACT

The aim of this work is to show the interest in using the deterministic fractal structures in the building of specific condensers compared to traditional plans condensers. Research relates on MOS condensers of which one of the plates is of fractional dimension. In the case of this work, it is about fractal tree of dimension 1.46 and Sierpinski carpet of dimension 1.89. The capacitive behavior of these particular condensers in which one of the plates is of fractional dimension is compared to traditional plane plate condensers. This study made it possible to note that MOS capacitors with fractional dimension have interests other than the value of the capacities they bring back but on the weakness of the dielectric constant. The study presented here is on the one hand, the development of the technological process of realization of the samples. On the other hand, the extraction of the capacities values of the samples previously mentioned above that are compared with those of the control plans capacities.

Key words: Fractal, fractional dimension, condenser, MOS technology, C (v) measurement

INTRODUCTION

Fractal structures are characterized by a geometric self-similarity and fractional dimension (Le-Mehaute, 1990). The study of the electrical model of the input impedance of these structures allows on the one hand to highlight a particular behavior (Niklasson, 1993) called constant phase angle or CPA on the argument curve. On the other hand, it reveals on the frequential evolution module curve of the aforesaid impedance (Haba *et al*., 1998) a fractional slope zone.

The unique characteristics of these structures namely self-similarity and fractional dimension "D_f" confer specific physical properties to these materials. It will be made in this work, a comparative study between a plane condenser of entire dimension and a plane condenser having one of the plates of, fractional dimension and the insulator, a silicon oxide (SiO_2). The deterministic fractal structures are used in several fields such electronics and the automatic for robust stabilization of feedback systems (Oustaloup, 1999; Joaquin *et al*., 2006; Haba *et al*., 2008). They are also found in the areas of mathematics and electrical modeling (Radwan *et al*., 2011; Shamim *et al*., 2011), in the field of microwave antennas (Parron *et al*., 2001; Canet and de Haro, 2004) but almost none is used in the manufacture of MOS capacity. One wants starting from the technological process of manufacturing capacitors on silicon (Haba *et al*., 1997), to carry out specifics MOS capacity with characteristics properties other than those with a capacity of conventional MOS.

This study is dedicated to the study of the behavior of C as function of V, for capacitive MOS structures for which one of the plates has fractional dimension and to compare them with a capacitor of the kind in conventional plane plates. This has been realized by measuring C(V) and the impedance, from which, it was deduced the capacitors values brought back by each structure and they were compared with the values returned by the control plans capacitors.

GEOMETRICAL CHARACTERISTICS OF PATTERNS OF THE STUDIED STRUCTURES

With a view to conducting a good study, research has brought about the structures of the fractal tree (Fig. 1) with a dimension of D_f = 1.465 and in those of the Sierpinski carpet (Gouyet, 1992) (Fig. 1) with a dimension of D_f = 1.893; both extracted from the following relation:

$$D_f = \frac{\log (N)}{\log (r)} \quad (1)$$

where, N is the number of parts created at each iteration and r, the ratio of reduction in length.

Sierpinski Carpet realization process: It is a non-ramified fractal structure with a particular "checkerboard" form. Its design principle is as follows: the initiating element is a full square with a side length L. Each side is divided by r = 3 forming 9 elementary squares. The generating element (structure having one iteration level) is obtained by removing the central square, as shown in the following Fig. 2.

To obtain the second level of iteration, one applies to the 8 remaining elementary squares the principle of generation describes above and so on for the following iterations. The number of elementary squares that the structure contains can be known at any iteration and that is possible by analyzing its generation process described as follows in Table 1.

Fractal tree realization process: The fractal tree is a ramified structure with a fractal dimension D_f (Gouyet, 1992) of 1,465 (N = 5 and r = 3) in contrast to Sierpinski carpet. The

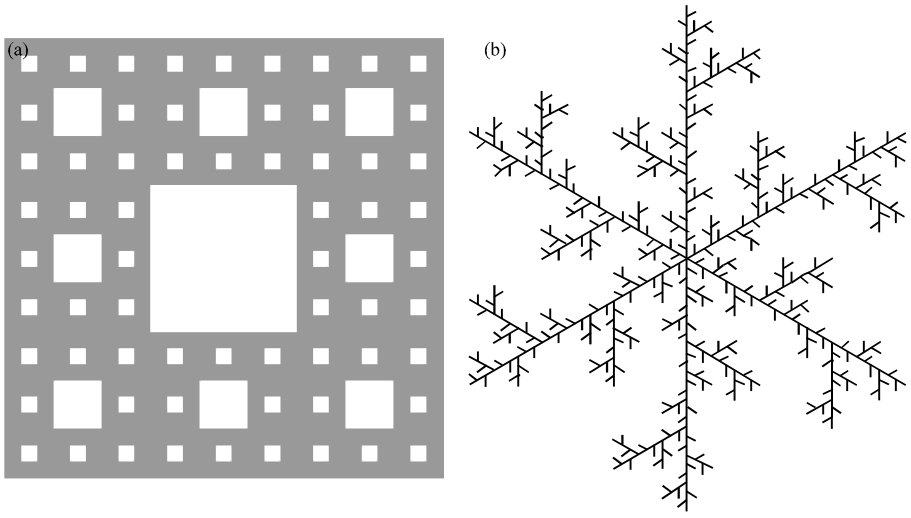

Fig. 1 (a-b): Patterns of the studied samples; (a): Sierpinski carpet and (b): Starry fractal tree

Table 1: Geometric characteristics of Sierpinski carpet

Iteration level	Number of elementary squares	Side length of an elementary square
1	8^1	$L_1=\frac{L}{3^1}$
2	8^2	$L_2=\frac{L}{3^2}$
3	8^3	$L_3=\frac{L}{3^3}$
-	-	-
n-1	8^{n-1}	$L_{n-1}=\frac{L}{3^{n-1}}$
n	8^n	$L_n=\frac{L}{3^n}$

Table 2: Geometric characteristics of the fractal tree

$l_n=\frac{L}{r^n}$	Length of a branch at iteration n
$N_{br}=5^n$	Total number of branches at iteration n

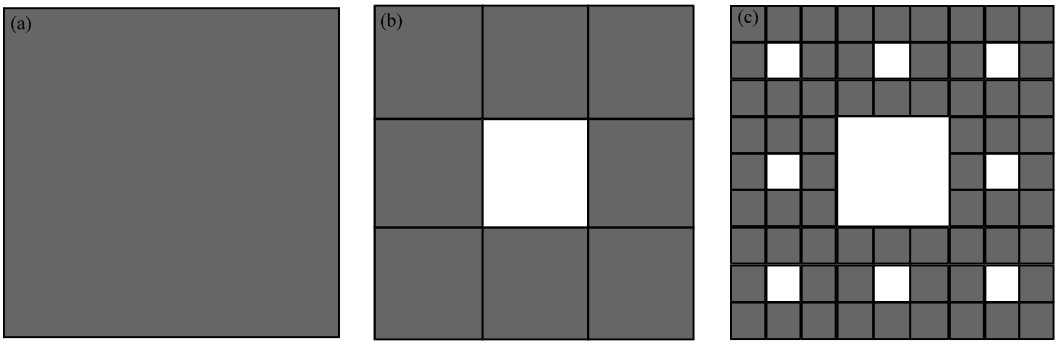

Fig. 2 (a-c): Construction process of Sierpinski carpet; (a): Initiator square; (b):Initiator element (The first level of iteration) and (c): Structure with two levels of iteration

structure under study has a construction process which can be described as follows: It begins with a base length $l_1 = l/3$. Then, one obtains, on each side of the initiator, 2 lateral segments of length l_1 at an angle θ with the initiator. The basic structure thus obtained is the generator, constituting the fractal tree at the iteration level 1. At this iteration level, the fractal tree disposes of 5 segments of identical length l/3. Applying the process of iteration to realize the tree, one obtains the fractal tree at iteration level 2 represented in Fig. 3. One can remark that the generator at iteration level 2 possesses the same structure as that at level 1 but reduced by a factor r = 3. On the other hand, the fractal tree corresponding to the iteration level 2 consists of N = 5 times more segments than that at level 1.

To shift the level of iteration n to the level of iteration n+1, is applied to all segments generated in previous iteration, the generation process described above. The characteristics related to the number and to the length of branches at a given iteration are defined in the following Table 2.

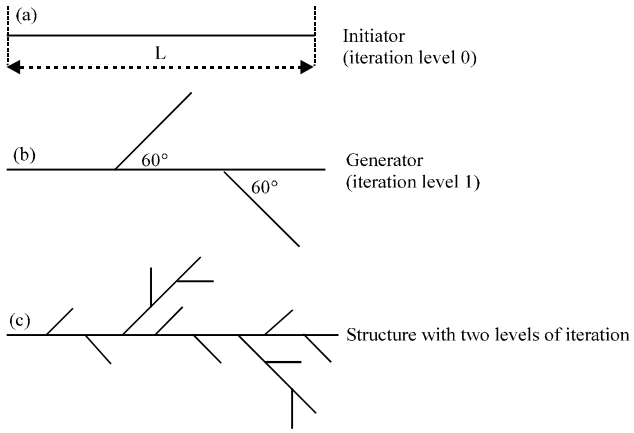

Fig. 3 (a-c): Construction process of the fractal tree; (a):Initiator (iteration level 0); (b): Generator (iteration level 1) and (c): Structure with two levels of iteration

TECHNOLOGICAL PROCESS OF MAKING STRUCTURES CONSIDERED

The different samples studied were made with the technique of buried structures using three mask levels which are: Pattern without contact studs (1st level), pattern with contact studs (2nd level) and contact studs without pattern (3rd level). The contact studs are the interconnection elements with the test circuit. For manufacturing, one begins by making grow on a naked substrate (P type, $N_A = 1.10^{15}$ cm^{-3}) a thick oxide called field oxide. This oxide will protect these different structures against possible deposition of impurities which may appear on the edges of the samples. One can note that these impurities can generate in these places phenomena conduction or leakage (Fig. 4a). This is followed by a photoetching of the fractal patterns in the oxide with the mask first level (Fig. 4a). It follows then grid oxidation followed by a deposit of Nidos (silicon layer doped by nitrogen Si_xN_y) (Scheid *et al*., 1994; Dehan *et al*., 1995) and of polysilicon which will be doped by Boron or phosphorus in order to fix its resistivity (Fig. 4a). In fact, it is the layer of Nidos which will act as protective shield by preventing the doping elements (phosphorus or boron) to pass through the layer of polysilicon to go and "pollute" the grid oxide coating, then the substrate. The last step in manufacture consists in metalizing the front and back faces then, in delimiting the contact studs by photoengraving with the 3rd level of mask. The different stages of technological process summarized in Table 3 make it possible to understand the advance followed to obtain our capacitive structures with fractional impedance (Haba *et al*., 2005) such as fractal tree and Sierpinski carpet.

Figure 4b is the final structure of each sample obtained at the end of the technological process described in Fig. 4a. It represents the result of the transformation of the naked silicon wafer having undergone steps 1 through 18 of the manufacturing process summarized in Table 3. The C(V) measurements were performed, using these samples (Fractal tree, Sierpinski carpet) with that structure.

It should be noted that one of the important phases of the technological process is the Radio Corporation of America cleaning (Kern and Puotinen, 1970) which precedes any phase of oxidation that occurs through the cycle in the diagram of Fig. 5. In effect, from this cleaning will depend the grid oxide quality of the MOS structure carried out. It eliminates a large proportion of charges that could have been trapped at the Si/SiO2 interface.

A description of the different stages of the oxidation cycle used during the manufacture of the samples is summarized in Table 4.

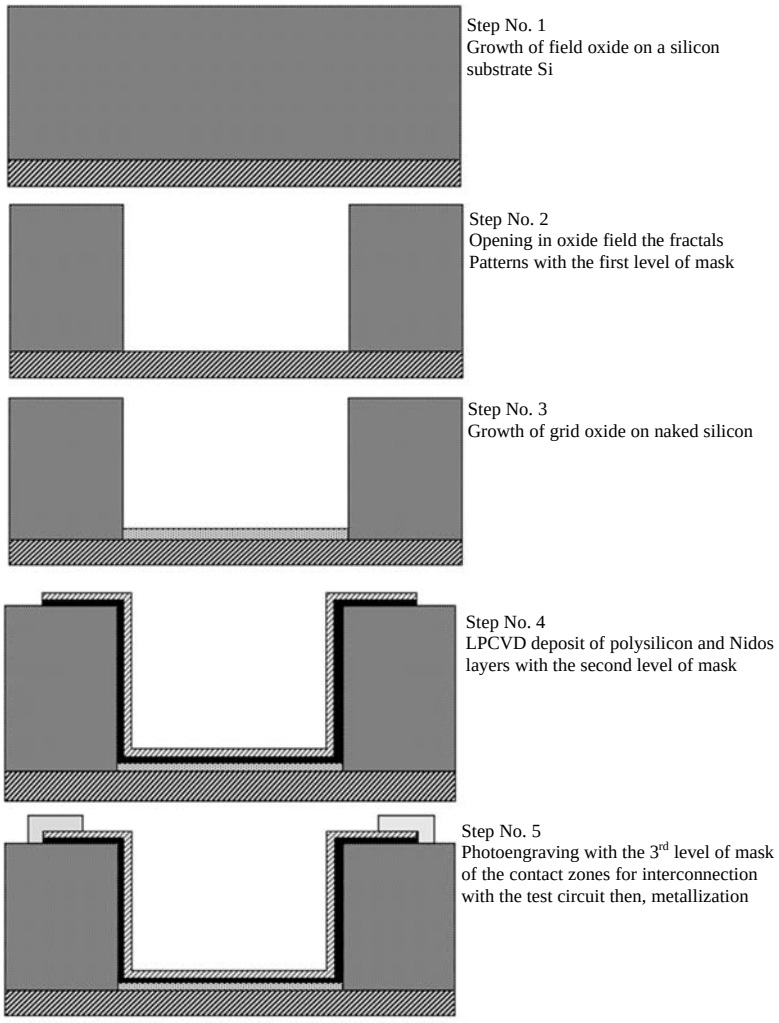

Fig. 4a: Different stages of the technological processes in manufacturing

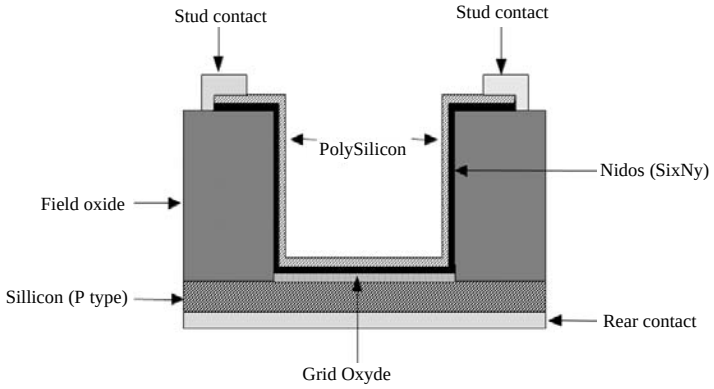

Fig. 4b: Final structure of the samples

Table 3: Description of the stages in manufacturing technology

Stages	Description of process phases
1	Cleaning and degreasing of the silicon substrate
2	Wet oxidation: E_{ox} = 7800 Å (it is the field oxide)
3	Photoetching mask No. 1 (resin>0) of different fractal patterns without studs: there is an opening pattern without the pads in the field oxide.
4	Chemical attack of the SiO_2 oxide on the fractal patterns and nowhere else
5	RCA cleaning (Si/SiO2 interface) in the bath-A=-A- A'-B-C
6	Grid oxidation with E_{ox} thickness = 195 Å : O_2 +N_2 + HCl
7	(L.P.C.V.D) deposit of Nidos (SiN0, 3) with a E_{nidos} thickness = 100 Å
8	(LPCVD) deposit of Polysilicon with E_{Poly} = 2600 Å
9	Polysilicon doping by Boron implantation to fix its resistivity
10	RTP annealing for 20 s at 1100°c
11	Photoengraving of different fractal patterns with studs (mask nE2 with resin>0)
12	R.I.E Attack (simultaneous) of Polysilicon, Nidos, SiO_2 layers and a thickness ε of Silicon (to make sure you have removed everything)
13	Front face metallization (aluminum) by sputtering with a thickness E_{Alu} = 8000 Å
14	Photoengraving (mask nE3 with positive resin) of the studs contact zones
15	Aluminum attacks: there will be Aluminum only on the studs contact zones
16	R.I.E attacks of the back face to eliminate the residues being able to be there
17	Back face metallization (Aluminum) with a thickness E_{Alu} = 8000 Å
18	Annealing for 20 min at 450 E c for a good ohmic contact of the studs interconnection of front and rear faces

Cleaning process Si/SiO2 interfaces developed by radio corporation of America. LPCVD: Low pressure chemical Vapor Disposition

Table 4: Grid oxidation cycle of the samples

	Description of the oxidation phases cycle
Phase (1)	Represents the temperature of the oven before oxidation (600 °)
Phase (2)	Rising oven in temperature during 30' to 900°C under nitrogen
Phase (3)	Stabilization of the oven for 5 'in pure nitrogen
Phase (4)	Oxidation itself during 2hrs
Phase (5)	Stabilization of the oven during 15' in pure nitrogen
Phase (6)	Oven rises in temperature during 15' at 1050°c
Phase (7)	Maintaining oven temperature under nitrogen for 30'
Phase (8)	Lowering the temperature of the oven for 1 h 30 'under nitrogen at 600°c
Phase (9)	Represents the oven temperature after oxidation (600°)

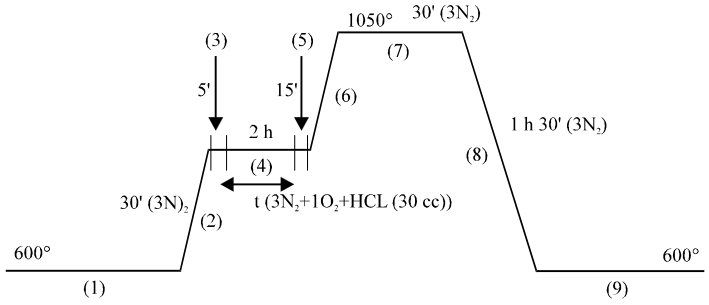

Fig. 5: Grid oxidation cycle of the samples

CHARACTERIZATION OF THE SAMPLES BY C (V) MEASUREMENT

The characterization of the samples takes place on a bench of low frequency measurement (LF) consisting of an automatic machine of test under points SET TC550 composed of a command and

control power station associated with a type HP 4284A capacitance meter on which impedance Z (F) and capacity measurements will be done according to the voltage (measurement in C (V)).

The major ranges of measurements of this bench are:

- Frequency F: From 20 Hz to 1 MHZ
- Voltage V: From -40V to +40V
- Capacitor C: From 10^{-15} to 10^{-5} F
- Impedance Z: From 10^{3} ohms to 10^{9} ohms

The capacitance-voltage measurements were done in low frequency regime (LF = 1 KHz) with a sinusoidal signal of 100 mV of amplitude. In high frequency regime (HF = 1 MHZ), measurements were made with a sinusoidal signal of 50 mV starting from the accumulation mode towards the inversion mode (Sarrabayrouse and Campabadal, 1990). The shape of the characteristic in C (V) of a control capacitor with plane plates (50.10^{-4} cm2 of surface) that we obtained is shown in Fig. 6. These measurements give access to many electrical parameters of the MOS capacitor such as: oxide thickness D_{ox}, resistance series * R_b + due to the volume of silicon and the back face contact when this one disturbs measurement, Doping semiconductor N_{dop}, the flat band voltage V_{FB}, surface potential ϕ_s according to the tension Vg applied, the distribution density of states surface N_{SS} and the fixed charges Q_{OX} in the oxide.

The measurements made out of C (V), not only make it possible to know the voltage range in which one can use the samples without risk of destroying but also allow us to check if the technological process of realization matches with the specifications.

Evaluation of some parameters: C_{ox}, D_{ox} and N_{dop}: The capacitance of the oxide layer of a MOS capacitor is given in one relation by Prom (1989) based on several important parameters. These are C_{max}, C_{sc}, ϕ_{so}, D_{ox} and ε_o where:

- C_{max} is the maximum capacity measured in high frequency
- C_{sc} the capacitance of the semiconductor
- ϕ_{so} the maximum surface potential in accumulation mode
- ε_o the permittivity of empty space and ε_{ox}, the constant dielectric of the oxide

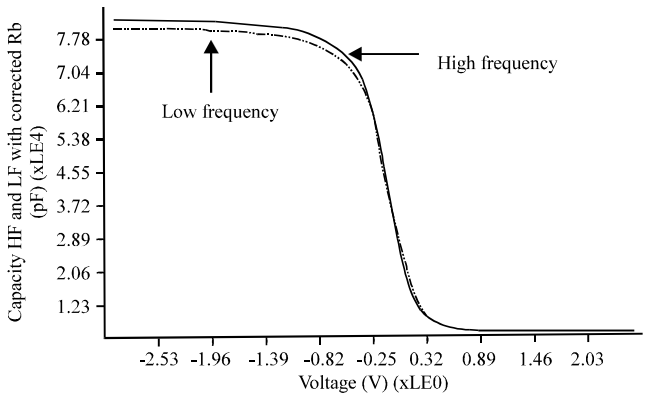

Fig. 6: Measure C (Vg) of a test capacity at low and high frequency

The same equation gives us another relationship between C_{ox} and D_{ox}. By knowing one of the parameters, it was possible to evaluate the other one. The doping of the semiconductor is determined from the curve C (V) obtained at high frequency (1 MHZ). The capacity of the space charge of the semiconductor which is defined by Kar and Dahlke (1972) in another relation allows the extraction of the expression of doping N_{dop}.

Measurements in C (V) of the structures of Sierpinski carpet and fractal tree: The study in this part is to study the curves of measurements in C (V) of the capacitive MOS structures of which one of the plates has fractional dimension and to compare them with conventional capacitors with plane plates. To do this, one will try to see if the relationship below is checked in the case of the structures of fractional order:

$$C_{acc} = C_{ox} \frac{\varepsilon_C . \varepsilon_{ox} . S}{D_{ox}} \quad (2)$$

With ε_0 the permittivity of empty space, ε_{ox}, the dielectric constant of the insulator and D_{ox}, the oxide thickness. The curves reflecting their electrical behavior are represented on the graphs of Fig. 7 and 8. Electrical measurements were performed from accumulation areas towards depletion areas on the two samples whose geometrical characteristics are mentioned in Table 5.

This table summarizes geometrical dimensions of the structures carried out for the study. S_1 is the elementary surface of a segment in the case of the fractal tree and an elementary square in the case of the Sierpinski carpet. Concerning S_2, this one represents the total surface of a branch of star comprising 3125 elementary segments. Being given that the complete structure of the fractal tree

Table 5: Geometrical characteristics of the samples

Structures	Geometrical dimension of an elementary rectangle	Geometrical characteristics for each sample
Fractal tree	L = 40 μm et l = 10 μm	S_1= 4 10^{-6} cm^2 = surface of a segment
		$S_2 = S_8 \times 5^5$ = 12.5 10^{-3} cm^2 = surface of a branch of the star
		$S_3 = S_2 \times 6$ = 75 10^{-3} cm^2 = surface of the 6 branches of the star
Sierpinski carpet	L = l = 40 μm	S_1= 16 10^{-6} cm^2 = surface of an elementary square
		$S_2 = S_1 \times 8^5$ =524.3 10^{-3} cm^2 = total area of the structure

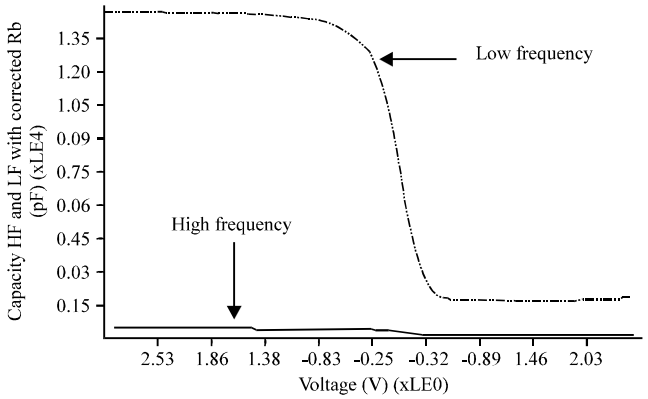

Fig. 7: Curve C (V) of a MOS capacitor of which one of the plates is the fractal tree with 5 levels of iteration

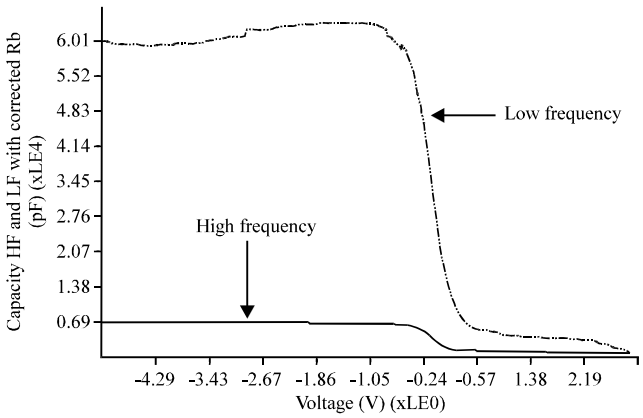

Fig. 8: Curve C (V) of a MOS capacitor of which one of the plates is the Sierpinski carpet with 5 levels of iteration

Table 6: Comparison of oxide thicknesses calculated and measured of two MOS structures with one plate of fractional dimension (accumulation mode)

Parameter	Sierpinskicarpet	Fractal tree
Surface of the studied structures	524.3 10^{-3} cm^2	12.5 10^{-3} cm^2
C_F (1 KHz) measured	62100 pf	1500 pf
C_F (1 MHZ) measured	6900 pf	75 pf
D_{ox} (1 KHz) calculated	291.4 Å	287.6 Å
D_{ox} (1 MHZ) calculated	2622.6 Å	5752.5 Å
D_{ox} measured (1 KHz et 1 MHZ)	217 Å	206 Å

comprises 6 branches, then S_3 represents the total surface of the sample having 5 levels of iterations. With regard to the Sierpinski carpet, S_2 represents the total surface of the sample comprising 32768 elementary squares.

Measurements were made at 1 KHz and at 1 MHZ. One cannot on the two curves obtained at 1 KHz that the accumulation mode and the depletion mode are done normally. On the other hand, when the frequency is at 1 MHZ, there is a very important series resistance which hides all the electrical behavior of the various structures. This shows experimentally that, one cannot bring back the surface of these structures to a single surface as it is possible in the case of a capacitor with plane plates (see curve in C (V) measurement of the test condenser).

The C (V) measurements technic at the frequencies of 1 KHz and 1 MHZ on test capacitors present on each substrate in accumulation mode have allowed to know exactly the real thicknesses D_{ox} of oxide present on each substrate. The same measurements also make it possible to extract the value of the capacities C_F brought back by each sample. The theoretical calculation of the thickness from the Eq. 2 is summarized in the Table 6.

One can note that from the linear relationship previously defined Eq. 2, one obtains oxide thickness values completely disproportionate compared to those obtained by measurement. The fact of obtaining too high oxide thicknesses and especially at high frequency (1 MHZ), leads us to say that these MOS capacitors cannot be described by a first order linear law (Haba *et al*., 2007).

Now, let us try to compare at equal surface and always in accumulation mode, two types of condenser such as one has two plane plates and the other has one of its plates of fractional dimension. To do this, one will choose the two structures mentioned above and then, one will

Table 7: Compare for the same surface of the plates, the equivalent capacitor C_{PEQ} and the capacitor of which one of the plates is of fractional order (F_C)

Parameters	Sierpinski carpet	Fractal tree
Surfaces of plates of capacitors	524.3 10^{-3} cm^2	12.5 10^{-3} cm^2
Thickness D_{ox}	217 Å	206 Å
C_F (1 kHz)	62.1nf	1.5nf
C_F (1 MHZ)	2.62nf	0.75nf
C_{Peq}	83.4nf	2.1nf

calculate on the basis of relation (2), the equivalent plane capacity as summarized in the following Table 7.

As in reference to the Eq. 2, this table presents the value of the C_{Peq} capacities which would be given by a plan condenser having same surfaces and the same oxide thickness.

On equal surface, one can note that whatever the work frequency, the value of the capacitor with plane plate is always greater than the capacitor of which one of the plates is of fractional order. In terms of capacity of condenser, C_{Peq} presents the best assets. Regarding the capacity of the capacitor C_F, its use is equivalent to a standard capacitor:

- Made up with either smaller plates
- Or containing a dielectric whose ε_r is lower
- Or with a higher oxide thickness

By using this kind of condenser, one can neither gain in terms of surface, nor in terms of oxide thickness but rather in terms of low dielectric permittivity.

CONCLUSION

One can just see that the deterministic fractal structures obtained by microelectronic process have interests other than the value of the capacities they bring back compared with those of plans condensers. At equal surface, the capacity C_F behaves as a plane condenser having dielectric whose ε_r would be lower. Such a material with low dielectric permittivity would be recommended in the area of absorption or emission of electromagnetic fields. As a matter of fact, the energy received by such a material is transformed into another form that is to say, in heat; which limits the power of the reflected waves.

So, one of the fields of application would be the field of radar and thus, of the stealth which will be the subject of future research.

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