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Logic Circuits and Gates in Pre A*-Algebra

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ABSTRACT

This study on algebraic structure of Pre A*-algebra. We define logic circuits and gates in Pre A*-algebra. We give truth tables for two inputs.

Key words: Boolean algebra, Pre A*-algebra, logic circuits, gates

INTRODUCTION

The study lattice theory had been made by Birkhoff (1948) and recently Pre A*-algebra had been studied by Chandrasekhararao *et al.* (2007). In a draft paper. The equational theory of disjoint alternatives, Manes (1989) introduced the concept of Ada, (A, Λ, v, (-)', $(-)^{\pi}$ 0, 1, 2) which however differs from the definition of the Ada by Manes (1993), While the Ada of the earlier draft seems to be based on extending the If-Then-Else concept more on the basis of Boolean algebras, the later concept is based on C- algebra (A, Λ, v, (-)~) introduced by Guzman and Squir (1990).

Koteswara Rao (1994) firstly introduced the concept of A*-algebra (A, Λ, v,*,(-)~, $(-)^{\pi}$ 0, 1, 2) and studied the equivalnence with Ada by Manes (1989), C-algebra by Guzman and Squier (1990) and Ada by Manes (1993) and its connection with 3-ring, stone type representation and introduced the concept of A*-clone and the If-Then-Else structure over A*-algebra and ideal of A*-algebra. Venkateswara Rao (2000) introduced the concept Pre A*-algebra (A, Λ, v, (-)~) analogous to C-algebra as a reduct of A*-algebra. Koteswara Rao and Venkateswara Rao (2003) studied about the algebraic structures of Boolean algebras and A*-algebras and the methods of generating A*-algebras from Boolean algebras and vice-versa. Koteswara Rao and Venkateswara Rao (2004) investigated about Prime Ideals and Congruences in A*-algebras. Koteswara Rao and Venkateswara Rao (2005) obtained the well-known Cayley theorem for A*-algebras. Koteswara Rao and Venkateswara Rao (2008) introduced the concept of A*-Modules and If-Then-Else Algebras over A*-algebras. Satyanarayana *et al.* (2009) studied extensively some structural compatibilities of Pre A*-algebra. Venkateswara Rao and Srinivasa Rao (2009) observed that Pre A*-algebra as a poset.

In this study, we define logic circuits and gates in Pre A*-algebra. We give truth tables for two inputs.

Definition: An algebra (A, Λ, v, (-)~), where A is non-empty set, Λ(meet), Λ(join) are binary operations and (-)~ (tilda) is a unary operation satisfying.

(a) $x^{\sim\sim} = x, \forall, x \in A$, (for all x belongs to A)
(b) $x \Lambda x = x, \forall, x \in A$
(c) $x \Lambda y = y\ x, \forall, x, y \in A$
(d) $(x \Lambda y)^{\sim} = x^{\sim} \text{ v } y^{\sim}, \forall\ x, y \in A$
(e) $x \Lambda (y \Lambda z) = (x \Lambda y) \Lambda z, \forall\ x, y, z \in A$
(f) $x \Lambda (y \text{ v } z) = (x \Lambda y) \text{ v } (x \Lambda z), \forall x, y, z \in A$
(g) $x \Lambda y = x \Lambda (x^{\sim} \text{ v } y), \forall x, y, z \in A$ is called a Pre A*-algebra

Example: 3 = {0, 1, 2} with operations Λ, v, $(-)^{\sim}$ defined below is a Pre A*-algebra.

Λ	0	1	2
0	0	0	2
1	0	1	2
2	2	2	2

v	0	1	2
0	0	1	2
1	1	1	2
2	2	2	2

x	$x^{\sim}$
0	1
1	0
2	2

Note: The elements 0, 1, 2 in the above example satisfy the following laws:

(i) $2^{\sim} = 2$
(ii) $1 \Lambda x = x$ for all $x \in 3$
(iii) $0 \text{ v } x = x, \forall\ x \in 3$
(iv) $2 \Lambda x = 2 \text{ v } x=2, \forall\ x \in 3$

Example: 2 = {0, 1} with operations Λ,v, $(-)^{\sim}$ defined below is a Pre A*-algebra.

Λ	0	1
0	0	0
1	0	1

v	0	1
0	0	1
1	1	1

x	$x^{\sim}$
0	1
1	0

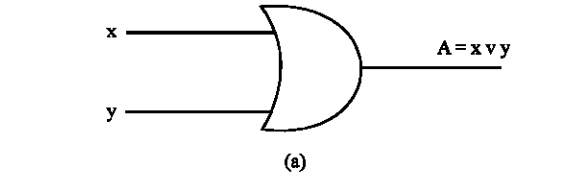
Note:
(1) (2, v, Λ, $(-)^{\sim}$) is a Boolean algebra. So, every Boolean algebra is a Pre A*-algebra.
(2) The identities (a) and (d) imply that the varieties of Pre A*-algebras satisfies all the dual statements of (a) to (g).

LOGIC CIRCUITS AND GATES IN PRE A*-ALGEBRAS

Logic circuits (Johnsonbaugh, 2001)

Definition: A computer switching circuit that consists of a number of logic gates and performs logical operations on data. Electronic circuits which process information encoded as one of a limited set of voltage or current levels. Logical circuits are the basic building blocks used to realize consumer and industrial products that incorporate digital electronics. Such products include digital computes, video games, voice synthesizers, pocket calculators and robot controls.

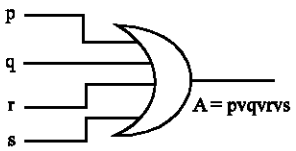
Logic circuits are also called logic networks, are structures which are built up from certain elementary circuits called logic gates. Each logic circuit may be viewed as a machine L which contains one or more input devices and exactly one output device. Each input device in L sends a signal specifically, 0, 1, or 2 to the circuit L and L proceses the set of {0, 1, 2} to yield an output. Accordingly, a sequence may be assigned to each input device and L processes the input sequences one digit at a time to produce an output sequence.



(a)

x	y	xvy
1	1	1
1	0	1
1	2	2
0	1	1
0	0	0
0	2	2
2	1	2
2	0	2
2	2	2

(b)



(c)

Fig. 1: (a-c) OR gate

First we define the logic gates and then we investigate the logic circuits.

Logic gates (Johnsonbaugh, 2001): There are three basic logic gates which are described below. We adopt the connection that the lines entering the gate symbol from the left are input lines and the single line on the right is the output line.

OR gate: Figure 1a-c show an OR Gate with inputs x and y and output A = x v y, where V is defined by the truth table in Fig. 1b.

Thus the output A = 0 only, when input x = 0 and y = 0, otherwise A = 1 or 2 gate may have mere than two inputs Fig. 1c shows an OR gate with four inputs p, q, r, s and output A = pvqvrvs The output A = 0 if and only if all the inputs are 0.

Suppose for instance, the input data for the OR gate in Fig. 1c are the following sequences:

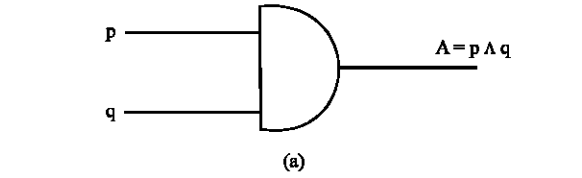
P = 1 0 2 0 1 2
q = 0 0 1 0 0 1
r = 2 1 0 0 0 2
s = 0 1 2 0 1 0
pvqvrvs = 2 1 2 0 1 2

The OR gate only yields 0 when all input bits are 0. This occurs only in the 4th position (reading from left to right). Thus, the output is the sequence A = 212012.

AND gate: Figure 2a-c show an AND gate with inputs p and q and output A = pΛq where multiplication is defined by pq, the truth table is shown in Fig. 2b. Thus the output A = 1 when input p = 1 and q = 1 otherwise A = 0 or 2.

Such as AND gate may have move than two inputs.

Figure 2c shows an AND gate with four inputs p, q, r, s and output A = pΛqΛrΛs. The output A = 1 if and only if all the inputs are 1.



p	q	p∧q
1	1	1
1	0	1
1	2	2
0	1	1
0	0	0
0	2	2
2	1	2
2	0	2
2	2	2

(b)

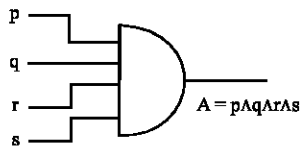
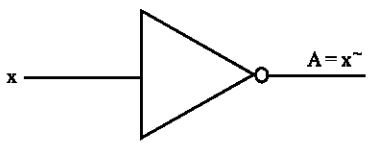


Fig. 2: (a-c) AND gate



x	x~
0	1
1	0
2	2

(b)

Fig. 3: (a, b) NOT gate

Suppose, for instance, the input data for the AND gate in Fig. 2c have the following sequences.

P = 1 1 1 0 2 1
q = 0 2 1 1 0 1
r = 2 0 1 2 2 1
s = 1 0 1 2 0 1
p∧q∧r∧s = 2 2 1 2 2 1

The AND gate only yields 1 when all input bits are 1. This occurs in 3rd and 6th positions. Thus, the output in the sequence 2 2 1 2 2 1.

NOT gate: Figure 3a and b show a NOT gate, also called a complement, with input x and output $x^{\sim}$ where complement denoted by the ~, in defined by the truth table in Fig. 3b. The value of the output $A = x^{\sim}$ is the complement of the input x.

i.e., $x^{\sim} = 1$ when $x = 0$
$x^{\sim} = 0$ when $x = 1$
$x^{\sim} = 2$ when $x = 2$

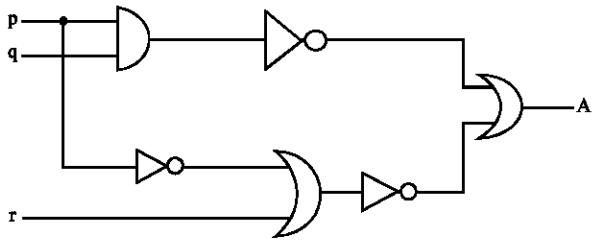


Fig. 4: Logic circuit with inputs p, q, r and output A

We emphasize that a NOT gate can have only one input, whereas the OR ad AND gates may have two or more inputs.

Suppose, for instance a NOT gate is asked to process the following three sequences.

$$A_1 = 0\ 2\ 0\ 0\ 0\ 1$$
$$A_2 = 1\ 0\ 2\ 0\ 0\ 1$$
$$A_3 = 2\ 0\ 1\ 0\ 0\ 1$$

The NOT gate changes 0 to 1, 1 to 0 Note that 2 does not changes. Thus,

$$A_1^{\sim} = 1\ 2\ 1\ 1\ 1\ 0$$
$$A_2^{\sim} = 0\ 1\ 2\ 1\ 1\ 0$$
$$A_3^{\sim} = 2\ 1\ 0\ 1\ 1\ 0$$

are the three corresponding outputs.

Logic circuits: A logic circuit L is a well formed structure whose elementary components are the above OR and ad NOT gates. Figure 4 is an example of a logic circuit with inputs p, q, r and output A. A dot (.) indicates a place where the input line splits so that its digit signal is sent in more than one direction.

Working from left to right, we express Y interms of the inputs p, q, r as follows. The output of the AND gate is $p\Lambda q$ which is then negated to yield $(p\ q)^{\sim}$.

The output of the lower OR gate is $p^{\sim} v\ r$, which is then negated to yield $(p^{\sim} v\ r)^{\sim}$. The output of the OR gate on the right, with inputs $(p\Lambda q)^{\sim}$ and $(p^{\sim} v\ r)^{\sim}$ gives us our desired representation, that is,

$$A = (p\ \Lambda q)^{\sim}\ V\ (p^{\sim} v\ r)^{\sim}$$

Logic circuits as a pre A*-algebra: Observe that the truth tables for the OR and NOT gates are respectively identical to the truth tables for the propositions p v q (disjunction p or q) $p\Lambda q$ (conjuction p and q) and ~p (negation, not p).

The only difference is that 1, 0 and 2 are used instead of T, F and N (N for Neither True Nor False).

p	p	pvq	pvq
T	T	T	T
T	F	T	F
T	N	N	N
F	T	T	F
F	F	F	F
F	N	N	N
N	T	N	N
N	F	N	N
N	N	N	N

"p or q" "p and q"

p	~p
T	F
F	T
N	N

NOT P

Note that in Pre A*-algebra, "p and q", "p or q" are same when N appears as one of the truth value. Also ~p remains same when N is the truth value.

Propositions: Let P (p, q,.....) denote an expression constructed from logic variable p,q,... which take on the value True (T), False (F) Neither True Nor False (N) and the logical connectives Λ, V and ~, such an expression P (p, q,.....) will be called a proposition.

Theorem: Logic circuits form a Pre A* – algebra.

Since logic circuits form a Boolean algebra and hence form a Pre A*-Algebra.

Proof: The truth tables for the OR and NOT gates are respectively identical to the truth tables for the propositions p v q (disjunction, "p or q), p Λ q (conjunction "p and q") and ~p (negation, "not p"). the only difference is that 1 and 0 are used instead of T and F. Thus the logic circuits satisfy the same laws as do propositions and hence they form a Boolean algebra. The 2 is used instead of N (neither true nor false) in Pre A*-algebra. Thus the logic circuits satisfy the same laws as do propositions and hence they form a Pre A*-algebra.

AND-OR circuits: The logic circuit L which corresponds to a Boolean sum of products expression is called an AND-OR circuit. Such a circuit L has several inputs where:

- Some of the inputs or their complements are fed into each AND gate
- The outputs of all the AND gates are fed into a single OR gate
- The output of the OR gate is the output for the circuit L

The following illustrates this type of a logic circuit.

Figure 5 is a typical AND-OR circuit with three inputs p, q, r ad output A. We can easily express A as a Boolean expression in the inputs p, q, r as follows. First we find the output of each AND gate.

- The inputs of the first AND gate are p, q, r hence p Λq Λr is the output.
- The inputs of the second AND gate are p, q~, r hence pΛq~Λr is the output
- The inputs of the third AND gate are p~ ad q hence p~ Λq is the output

Then the sum of the outputs of the AND gates is the output of the OR gate, which is the output A of the circuit. Thus A = (pΛqΛr) v (pΛq~ Λr) v (p~Λq).

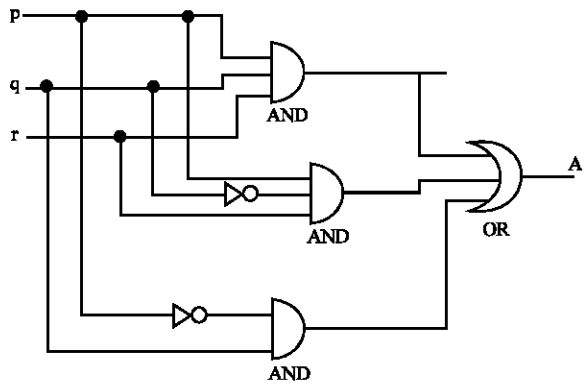
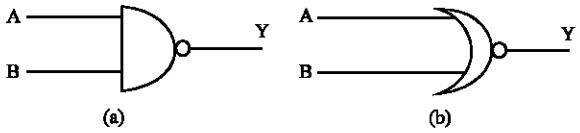


Fig. 5: Diagram of AND-OR circuit



A	B	NAND	NOR
1	1	0	0
1	0	1	0
1	2	2	2
0	1	1	0
0	0	1	1
0	2	2	2
2	1	2	2
2	0	2	2
2	2	2	2

(c)

Fig. 6: (a) NAND, (b) NOR gate and (c) Truth table

NAND and NOR gates: There are two additional gates which are equivalent to combinations of the above basic gates.

- NAND gate, shown in Fig. 6a is equivalent to an AND gate followed by a NOT gate
- NOR gate, shown in Fig. 6b is equivalent to an OR gate followed by a NOT gate

The truth tables for these gates (using two inputs A and B) appear in Fig. 6c. The NAND and NOR gates can actually have two or more inputs just like the corresponding AND ad OR gates. Furthermore, the output of a NAND gate is 0 if and only if all the inputs are 1 and the output of a NOR gate is 1 if ad only if all inputs are 0. also the output of a NAND and NOR gate is 2 if one of the input is 2.

Observe that the only difference between the AND and NAND gates and between the OR and NOR gates is that the NAND ad NOR gates are each followed by a circle (Fig. 7a, b). We can also use such a small circle to indicate a complement before a gate. For example, the Boolean expressions corresponding to the two logic circuits in Fig. 7 are as follows:

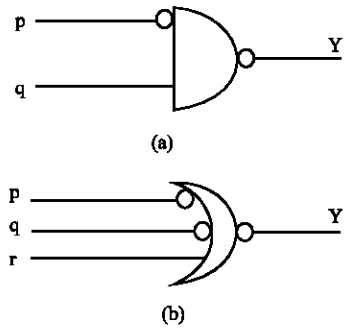


Fig. 7: (a) NAND and (b) NOR gate

- $Y = (p^{\sim} \Lambda q)^{\sim}$
- $Y = (p^{\sim} \text{ v } q^{\sim} \text{ v } r)^{\sim}$

REFERENCES

Birkhoff, G., 1948. Lattice Theory. Colloquium Publishers, New York.

Chandrasekhararao, K., J. Venkateswararao and P. Koteswararao, 2007. Pre A*-algebras. J. Inst. Mathe. Comput. Sci. Math. Ser., 20: 157-164.

Guzman, F. and C.C. Squier, 1990. The algebra of conditional logic. Algebra Universalis, 27: 88-110.

Johnsonbaugh, R., 2001. Discrete Mathematics. Pearson Education, Asia.

Koteswara Rao, P., 1994. A*-Algebras and if-then-else structures. Ph.D. Thesis, Acharya Nagarjuna University, Andhra Pradesh, India.

Koteswara Rao, P. and J. Venkateswara Rao, 2003. Boolean algebras and A-algebras. J. Pure Math., 20: 33-38.

Koteswara Rao, P. and J. Venkateswara Rao, 2004. Prime ideals and congruences in A*-algebras. Southeast Asian Bull. Math., 28: 1099-1119.

Koteswara Rao, P. and J. Venkateswara Rao, 2005. A Cayley theorem for A-Algebras. Sectunia Matematica, S1, F1, pp: 1-6.

Koteswara Rao, P. and J. Venkateswara Rao, 2008. A modules and If-then-else algebras over A-algebras. Int. J. Comput. Math. Appl., 2: 103-108.

Manes, E.G., 1989. The equational theory of disjoint alternatives. Personal Communication to Prof. N.V. Subrahmanyam.

Manes, E.G., 1993. Adas and the equational theory of if-then-else. Algebra Universalis, 30: 373-394.

Satyanarayana, A., J. Venkateswara Rao, K. Srinivasa Rao and U. Surya-Kumar, 2009. Some structural compatibilities of pre A-algebra. Afr. J. Math. Comput. Sci. Res., 3: 54-59.

Venkateswara Rao, J., 2000. On A-algebras. Doctoral Thesis, Nagarjuna University, A.P., India.

Venkateswara Rao, J. and K. Srinivasa Rao, 2009. Pre A*-algebra as a poset. Afr. J. Math. Comput. Sci. Res., 2: 73-80.