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Organic Field Effect Transistor with Silica Nanoparticles on Gate Dielectric

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ABSTRACT

The benefits of Organic Field Effect Transistors (OFETs), such as economical, large area fabrication and flexibility, have recently attracted much attention. Utilitarian transistors demand low threshold voltage, high mobility, large on/off ratio and stability. Innovation in organic semiconductors is crucial to obtaining these specifications. The requirement for high mobility and low operating voltages is the motivation for using high dielectric constant materials in Organic Field Effect Transistors (OFETs). In this study the fabrication and performance of an OFET with silica nanoparticle (dielectric constant of silica~3.9) as dielectric layer is reported. The device is fabricated with, bottom contact architecture with Poly (3-hexylthiophene) (P3HT) as active layer and aluminium as electrode.

Key words: Organic electronics, organic field effect transistor, conducting polymers, field effect mobility, dielectric materials, nanoparticles

INTRODUCTION

Organic field-effect transistors fabricated using polymers (Tsumura *et al*., 1988) and small molecules (Horowitz *et al*., 1992) emerged in the late 1980s and have been developed into an attractive cost-effective technology. Initially OFETs had considerable field-effect charge-carrier mobilities, μ_{FET} but was not on par with the inorganic field effect transistors. Rigorous experimentation leads solution-processed OFET advance towards (Sirringhaus, 2005) the field effect mobilities of amorphous silicon (a-Si). Encouraging examples (Crone *et al*., 2000) of organic active-matrix driving schemes for flexible and large-area flat-panel displays (Clemens *et al*., 2004) radio-frequency identification tags (McCulloch *et al*., 2006) sensors (Roberts *et al*., 2008) and ink-jet printed circuits (Spijkman *et al*., 2010; Rogers *et al*., 1999; Gelinck *et al*., 2000; Baude *et al*., 2003) have been demonstrated. OFETs have a layered structure consisting of a gate and source/drain electrodes, gate insulator and semiconducting layer as in Fig. 1. All of the components and interfaces are important for correct functioning of OFET.

The use of high-κ dielectric material for gate insulator improves the field effect mobility of the polymer semiconductor. Also, the high current density fills the trap at low gate potential. Therefore, this gives a high chance of achieving good voltage-current characteristics (Gamerith *et al*., 2007; Wang *et al*., 2004; Bernardi *et al*., 2001; Ramajothi *et al*., 2008) for operation of devices at low drive

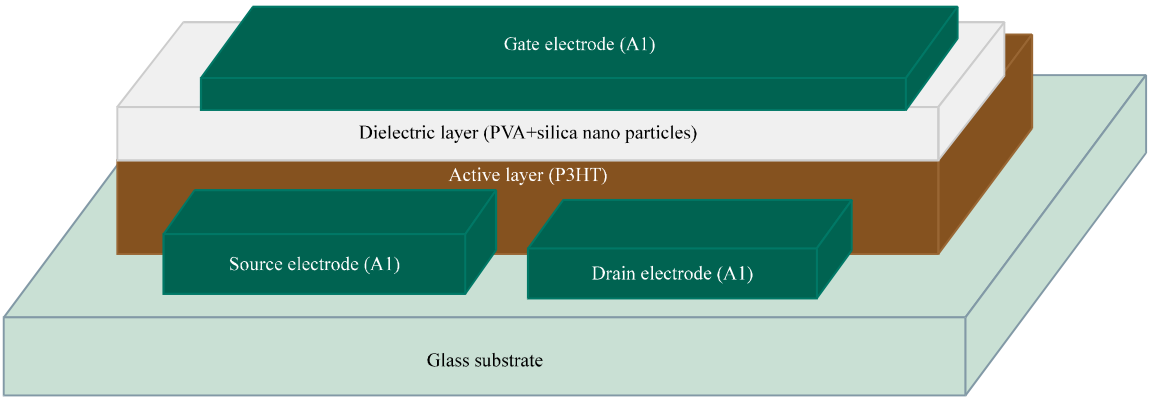

Fig. 1: Schematic representation of top-gate/bottom-contact OFET structure

voltage. This gives the motivation for innovations in dielectric materials while fabricating OFETs (Veres *et al*., 2004). The effect of modifying the gate dielectric, (PVA) with silica nanoparticles is investigated and the results are discussed.

For OFET device fabrication, top gate/bottom contact architecture is employed with a P3HT (Poly (3-hexylthiophene), as active layer. Wild application of regioregular P3HT (p-type (mobility = 10^{-4}-10^{-1}cm^2/V.sec) can be attributed to its ease of procurement and high mobility (Lee *et al*., 2010; Wang *et al*., 2003). Similarly (PVA) (Dennler *et al*., 2009; Lee *et al*., 2003; Kunugi *et al*., 2010; Sethuraman *et al*., 2008) is one of the most common and easily processable dielectric materials widely explored as gate dielectric in OFETs. Polyvinyl alcohol (PVA) is first dissolved in water followed by compounding it with an aqueous dispersion of silica nanoparticles to form the dielectric layer. The addition of silica nanoparticles is expected to improve the performance of OFET devices and this forms the major objective of this study.

MATERIALS AND METHODS

Glass substrate is cleaned using soap solution followed by acetone, then it is subjected to plasma treatment which increases the possibility for a better self-assembly of P3HT in a thin glass substrate (Machado and Hummelgen, 2012). After plasma treatment, 340 nm thick Al source-drain electrode layer was deposited under vacuum of below 1.5×10^{-5} mbar for 10 min using a shadow mask. High quality regioregular P3HT (degree of regioregularity ~99% and Mw~87000) purchased from Sigma Aldrich is dissolved in toluene with the weight percentage 10 mg mL^{-1} (Meng *et al*., 2006; Jiang *et al*., 2011). Drop casting using micro syringe is used to assemble RR-P3HT films over the electrodes. Drop casting is used since it has been reported (Tian *et al*., 2010; Weiss *et al*., 2007; Surin *et al*., 2006) that the mobility of P3HT films is higher than that made by spin coating. The mobilities obtained for drop-cast P3HT devices show better results when compared to spin coated devices.

PVA solution is made by dissolving and stirring 0.075 g of PVA and 1 mL of water at for 4 h. PVA and silica nanoparticles dispersed in water (2 mg L^{-1} mL) is mixed and sonicated for even distribution of particles throughout the volume. This is the modified PVA composite is drop cast over the active layer. Silica nanoparticles are synthesized by Stober Process (Wang *et al*., 2007; Ko *et al*., 2004; Cortes Escobedo *et al*., 2006; Milea *et al*., 2011; Singho and Johan, 2012) using TEOS (Tetraethyl orthosilicate-Si (OC2H5)4). Sonicate the mixture of TEOS and ethanol for

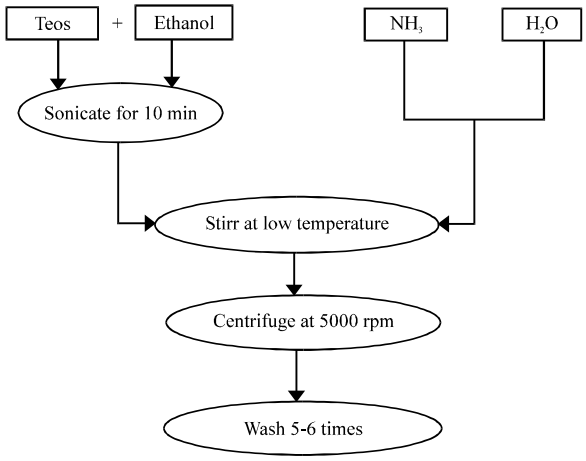

Fig. 2: Flowchart for Stober process

10 min. Mix this with aqueous ammonia solution by stirring at low temperature. Centrifuge this solution at 5000 rpm. Wash the centrifugate five to six times to get silica nanoparticles. Flow chart for Stober process is shown in Fig. 2. After the active layer is dried, aluminum is deposited as gate electrode using vacuum deposition in the same manner as in the case of electrode. The surface morphology of dielectric material and silica nanoparticles dispersed in water is observed by HITACHI SU6600 field emission Scanning Electron Microscope (SEM). Number-weighed size distribution of nanoparticles is evaluated at 25°C on a Malvern Zetasizer nano EZS90 using Dynamic Light Scattering (DLS).

The OFET performance characterization is carried out at room temperature. For electrical characterizations, Keithley 2400 Source Meter and Keithley 6517 B Electrometer/High Resistance Meter are used for measuring source-drain voltage, source-drain current and gate voltage, respectively. This setup is controlled by labview software with PC. Capacitance of the device is measured by impedance analyzer.

RESULTS AND DISCUSSION

SEM images (Fig. 3, 4) are used to evaluate the morphology of synthesized silica nanoparticles and the composite dielectric material. The SEM images also showed some evidence of slight aggregation and fusing. Particle size of nanoparticles is found to be 300 nm. Figure 5 shows SEM image of channel length. For calculations, average channel length was taken as 39 μm. Though, Fig. 6 shows a uniform distribution of number-weighed particle size, as measured from DLS, the average size of nanoparticles comes to 498.2 nm. Large size hydrodynamic shell might be the reason for this rather abnormally high average size of the particle. The large size of hydrodynamic shell, in turn, might be the affect of the non smooth and odd shaped particles besides the composition. Interparticle interaction and complex particle shape can also affect the numerical evaluation from DLS. Even a mere 1-2 vol.% of larger particles can significantly affect the DLS derived particle size distribution (Rahman and Padavettan, 2012). SEM images are free from this draw back being less susceptible to the larger aggregates.

While doing electrical characterization, OFET is functioned in the accumulation regime by providing positive bias. Drain electrode is connected to the positive terminal and source electrode

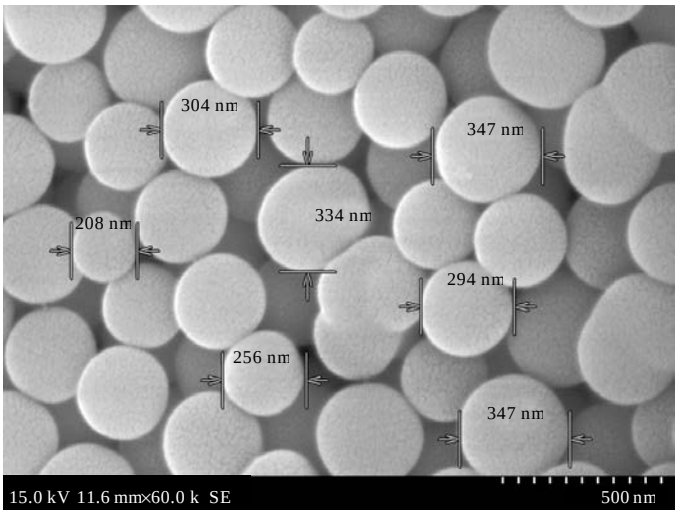

Fig. 3: SEM image of silica nanoparticles

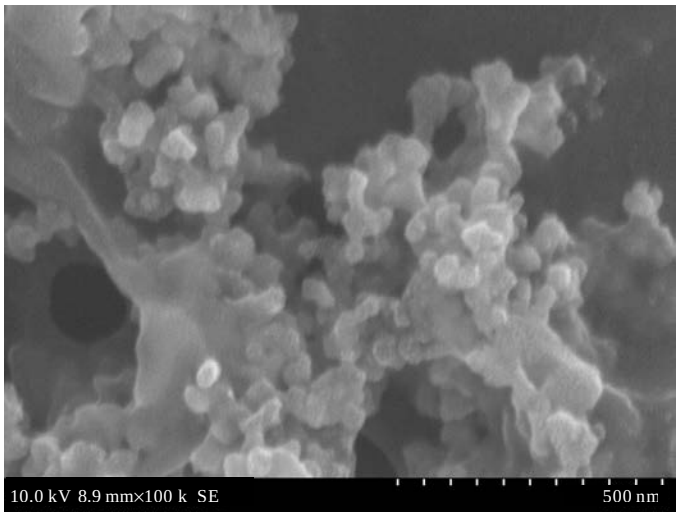

Fig. 4: SEM image of dielectric

is grounded. Figure 7 shows the relationships between I_{sd} and V_{sd} of different positive gate voltages. Mobility $\mu(cm^2\ V^{-1} sec^{-1})$ is an important parameter that can be deduced from I_{ds}-V_{ds} measurements in accumulation mode. It can be estimated from the gradient (g_m) of a trace of $I_{ds}^{1/2}$ as a function of V_g. Figure 8 shows the transconductance (g_m) of the fabricated devices. Active layer charge density decreases due to the decrease in V_g. These curves are a pattern for the depletion mode in positive V_g range. Transconductance value (g_m) of the devices can be calculated using the ratio of change in source drain current (ΔIds) to the change in gate source voltage (ΔV_g). Field effect mobility μ_{FET} and threshold voltage (V_T) can be calculated from the well known equation (Katzel *et al*., 2008).

$$\mu = \frac{g_m.L}{W.C_p.V_{ds}} \quad (1)$$

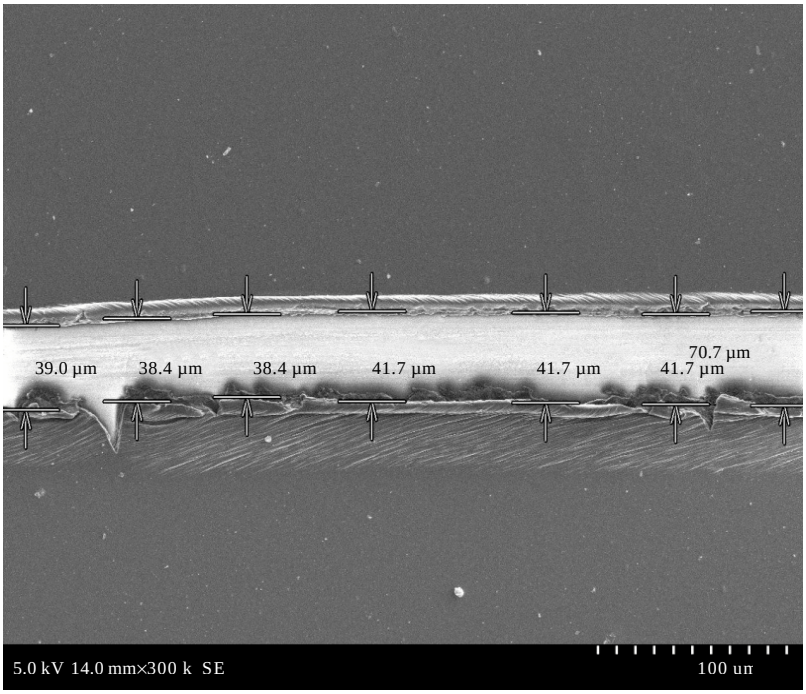

Fig. 5: Image of a critical dimension pattern pictured by SEM

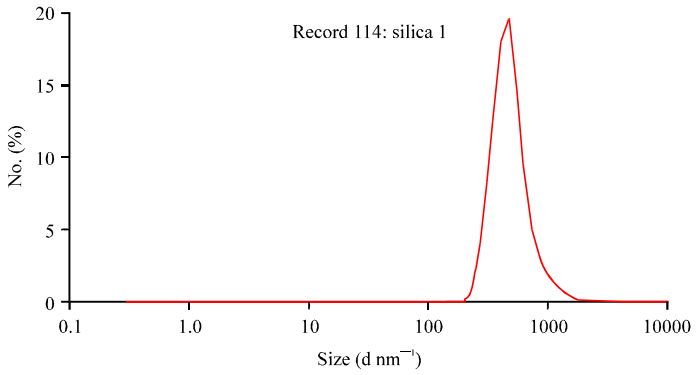

Fig. 6: Size distribution by number

$$I_{dss} = \frac{WC_p\mu(v_g - v_{th})^2}{2L} \quad (2)$$

The channel width (W) and channel length (L) are taken as 4 mm and 32 µm (Fig. 6), respectively and C_p(nF cm^{-2}) capacitance of the device. The field effect mobility (µ), V_T and I_{on}/I_{oft} ratio are 2.167×10^{-5} cm^2 V^{-1} sec^{-1}, 56 V and 0.25×10^2, respectively.

Capacitance variation as a function of frequency was taken using impedance analyzer to measure the dielectric characteristics of the device. The plate capacitance was measured to be 0.9×10^{-1}F/cm^2. In the case of FET, as positive gate voltage increases, source drain current decreases which is due to the negative charge induced in active channel with the help of positive gate bias voltages indicating p-type of FET operation in depletion mode. When gate source terminal is applied

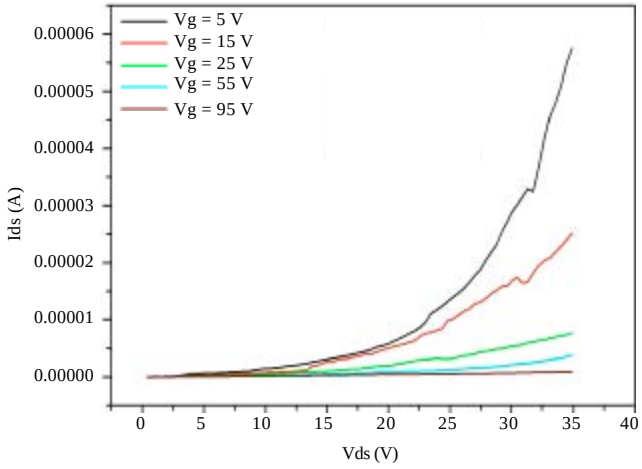

Fig. 7: Relationship between I_{sd} and V_{sd} upon sweeping positive gate voltage

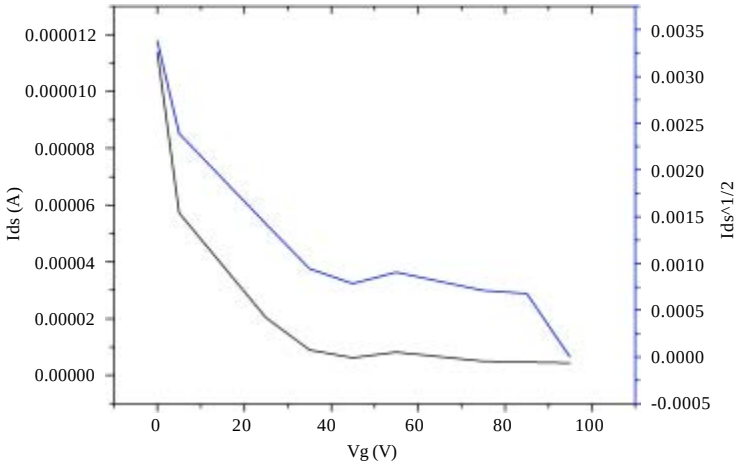

Fig. 8: Transconductance curve

a negative bias voltage, I_{sd} would increase. In these devices the positive bias voltage 0 to +95 to the gate source terminal and 0 to +40 bias voltages to source drain terminal, in the ohmic region. The device is found to have a turn off at +95 gate voltage. Further study in silica nanoparticles arrangement, optimization in channel length and use of layered structure in dielectric (Gupta *et al*., 2006) are promising for the improvement in the OFET characteristics.

CONCLUSION

An OFET with top gate/bottom contact architecture is fabricated with P3HT as semiconductor and PVA composite as dielectric. Mobility and I_{on}/I_{off} is found to be 2.167×10^{-5} cm^2 V^{-1} sec^{-1} and 0.25×10^2, respectively. Here, we initiated the study of incorporation of silica nanoparticles along with conventional PVA organic polymer as dielectric material. A comparable result for the field effect mobility, threshold voltage and I_{on}/I_{off} ratio is observed and reported in this study. Although, the obtained μ_{FET} is a sufficient value for the organic active layer, better characteristics will be

obtained with further optimization. Scope of this study can be extended to optimizing channel length, silica nanoparticles arrangement, layered structure for dielectrics and much more related fields.

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